

Siberia Block Diagram

Project code: 91.4Q601.001
PCB P/N : 48.4Q613.011
REVISION : 06248-1

System DC/DC TPS51120 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW +5V_SUS +3.3V_SUS +3.3V_RTC_LDO
System DC/DC SN0508073 44	
+PWR_SRC	+1.5V_RUN +1.25V_RUN
DDR2 DC/DC SN0508073 45	
+PWR_SRC	+1.8V_SUS +1.05V_VCCP
LDO TPS51100 47	
+1.8V_SUS	+0.9V_DDR_VTT
LDO MAX668 47	
+PWR_SRC	+12V_S

Battery Charger ISL88731 41	
INPUTS	OUTPUTS
+PWR_SRC	+VCHGR

CPU DC/DC ISL6260C 42, 43	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

PCB LAYER	
L1: TOP	
L2: GND	
L3: Signal	
L4: Signal	
L5: VCC	
L6: Signal	
L7: GND	
L8: BOT	

<Core Design>

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

BLOCK DIAGRAM		
Siberia		
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WWW.AliSaler.Com

CLOCK GEN CY28547

27M_SS/LCD96_100M SELECTION TABLE

BYTE 10

Bit5 S1	Bit4 S0	Spread Spectrum S[1:0]
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

BYTE 15

IO_VOUT[2,1,0]

Bit2	Bit1	Bit0	IO_VOUT[2,1,0]
IO_VOUT2	IO_VOUT1	IO_VOUT0	
0	0	1	0.3V
0	0	0	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSA	FSA		
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 9	Lane Reversal	Normal Mode(Lanes number in order) ★
CFG 16	FSB Dynamic ODT	Disabled
CFG 19	DMI Lane Reserved	Lane Reserved
CFG 20	Only PCIE or SDVO is operation ★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA	NO SDVO Card Present ★	SDVO Card Present

CFG 12	XOR/ALL-Z
CFG 13	Reserved
LL(00)	Reserved
HL(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HL(11)	Normal Operation

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	BT/UWB/Robson
LANE4	Express Card
LANE5	PPU card
LANE6	Giba Bit LOM

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/MediaCard	AD17	C D	1	1

USB TABLE

ICH

USB0	Ext Lift Side
USB1	Ext Back
USB2	Ext Right Side (Top)
USB3	Ext Right Side (Bottom)
USB4	3rd mini card
USB5	Camera
USB6	Express Card
USB7	BT
USB8	Gaming LCD
USB9	WWAN

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved. Rising Edge of PWROK.	Weak Internal PULL-DOWN. NOTE: This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWB BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h: bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05, VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL. Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit. (Offset: 3410h: bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up. If sampled low, the Flash Descriptor Security will be overridden. If high, the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap		
ICH_RST#p3	AZ_DOUT ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (default)
1	1	Set PCIE port config bit1

A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable	high = default
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (Default)

Integrated VccSus1_05, VccSus1_5, VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
Integrated VccLAN1_05 VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Default
	High=No Reboot

8.2K PULL HIGH

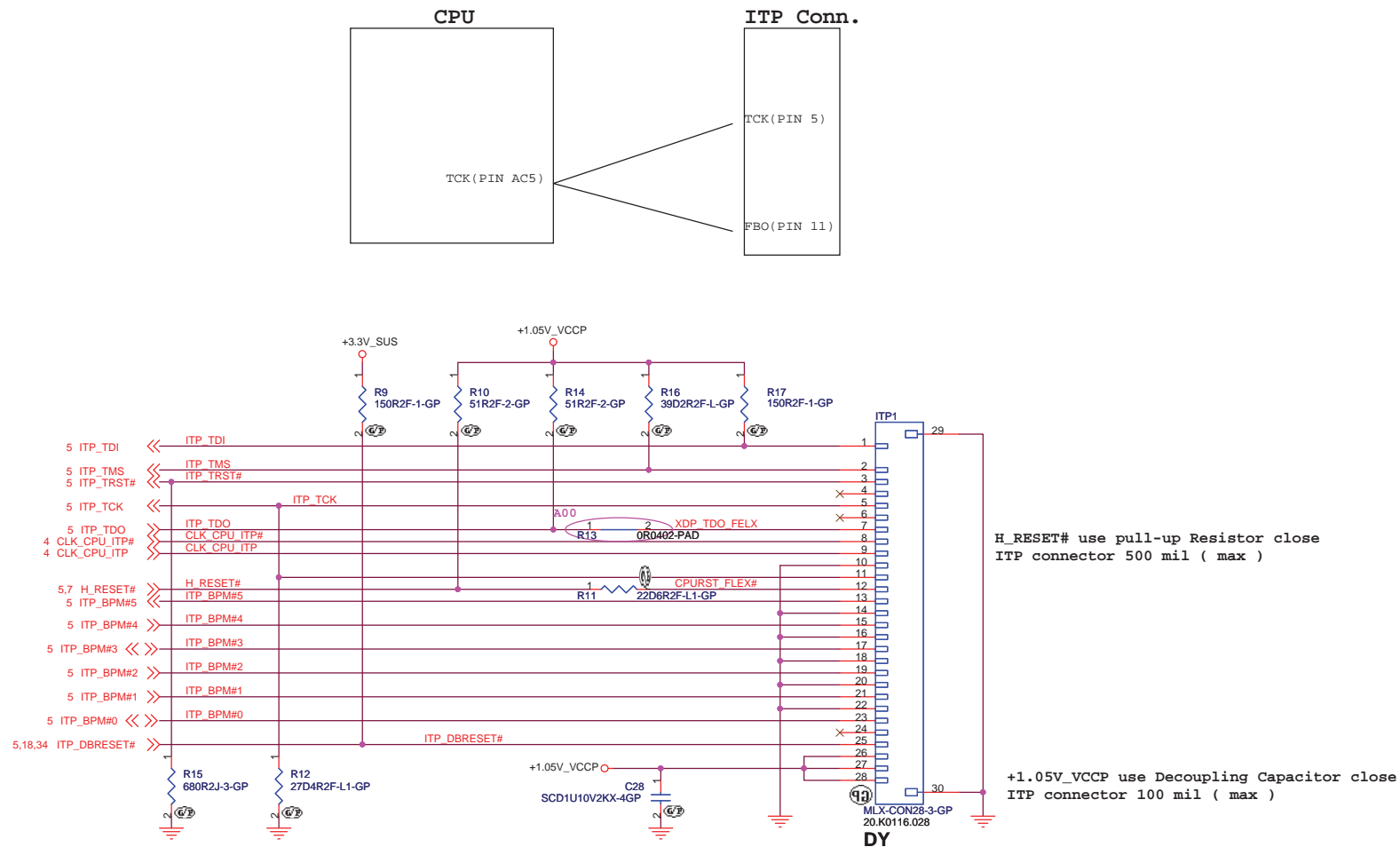
INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST0#	PULL-UP 13K

Core Design:



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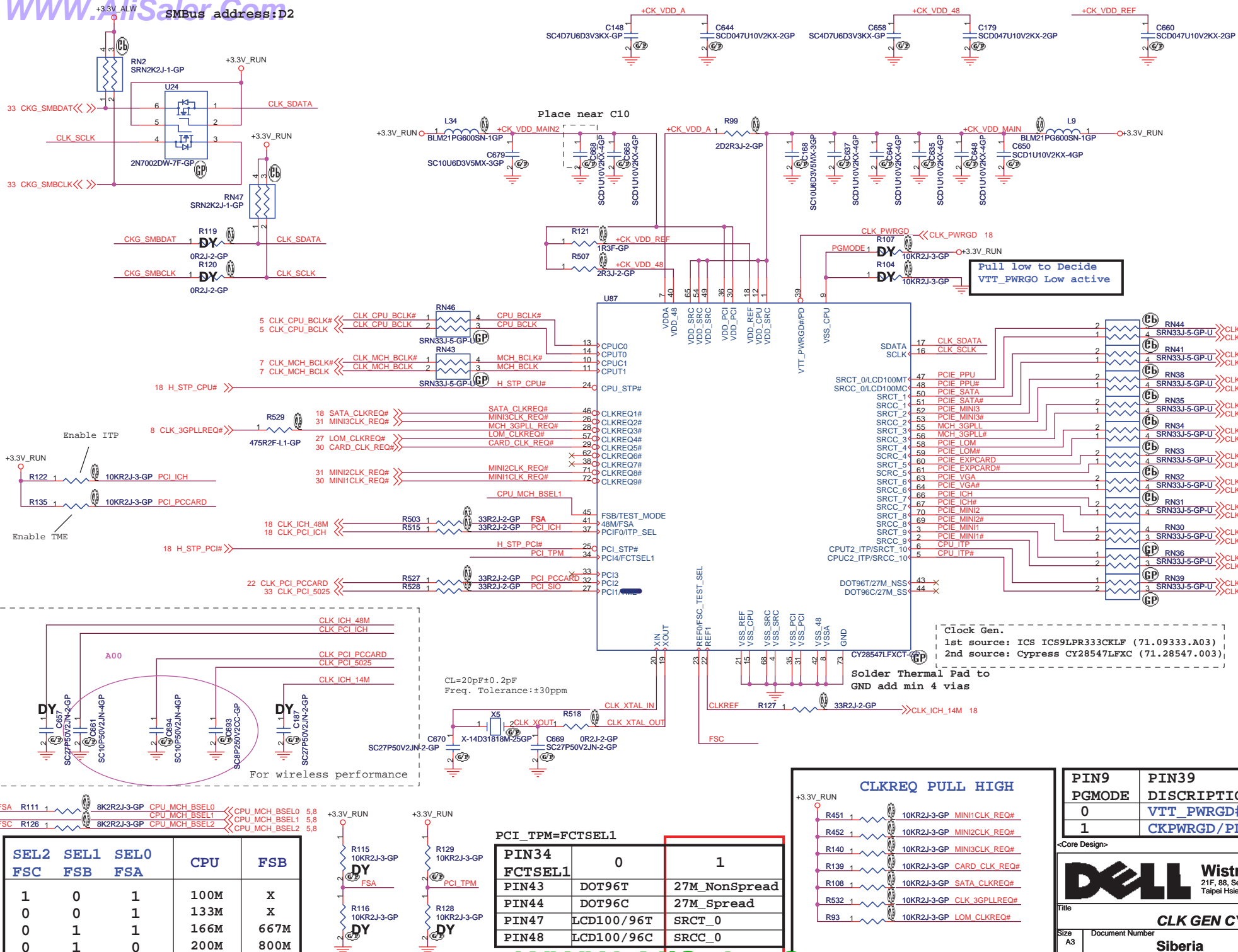
H_RESET# use pull-up Resistor close
ITP connector 500 mil (max)

+1.05V_VCCP use Decoupling Capacitor close
ITP connector 100 mil (max)

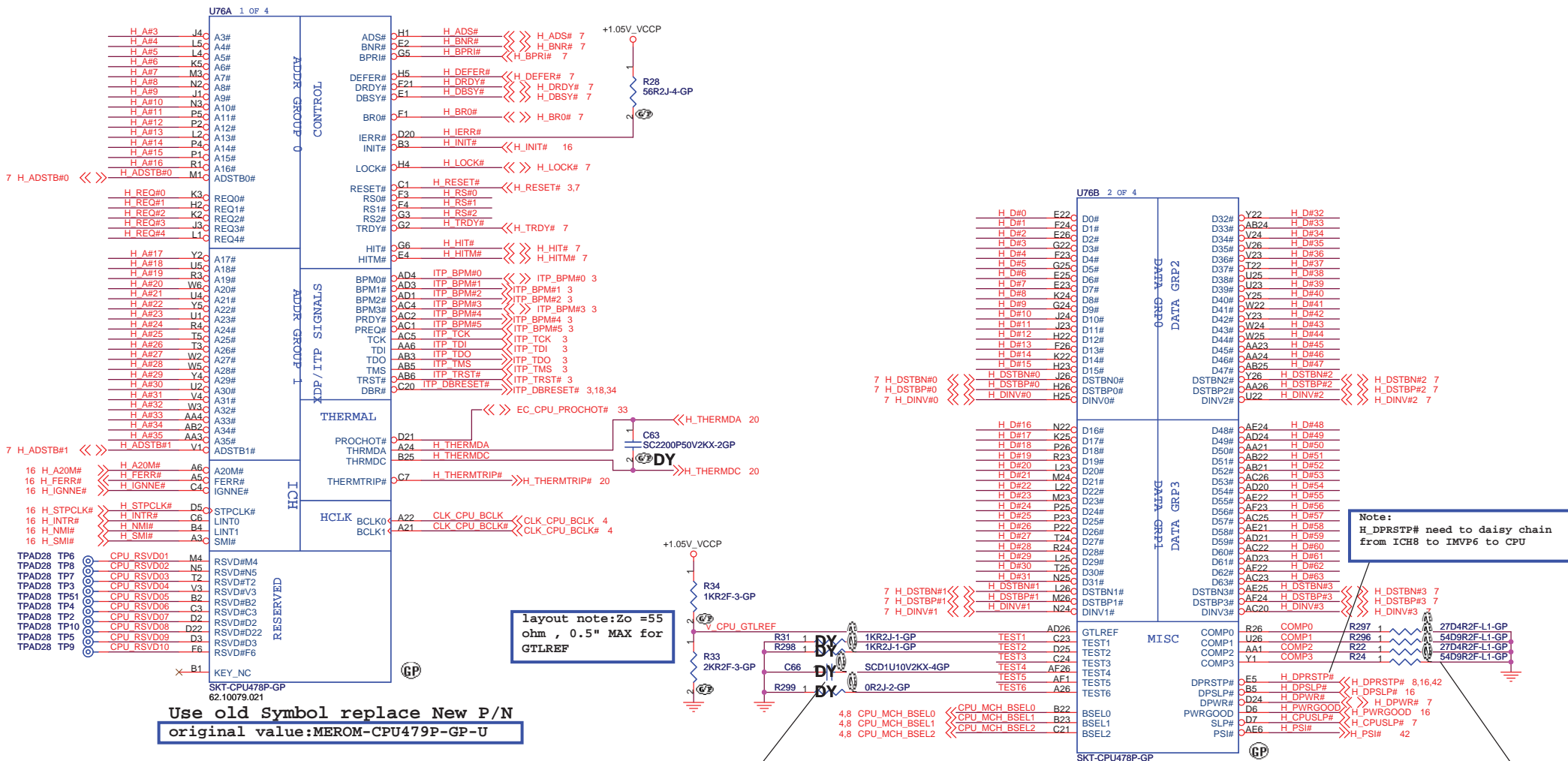
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Title			ITP Debug	
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H_D#[63..0] <<>> H_D#[63..0] 7
 H_A#[35..3] <<>> H_A#[35..3] 7
 H_REQ#[4..0] <<>> H_REQ#[4..0] 7
 H_RS#[2..0] <<>> H_RS#[2..0] 7



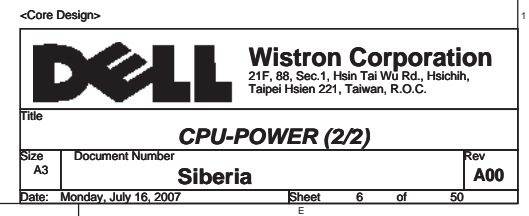
Use old Symbol replace New P/N
 original value:MEROM-CPU479P-GP-U

layout note:Zo =55
 ohm , 0.5" MAX for
 GTLREF

PLACE C66 close to the TEST4 PIN,
 make sure TEST4 PIN routing is
 reference to GND and away from
 other noisy signals

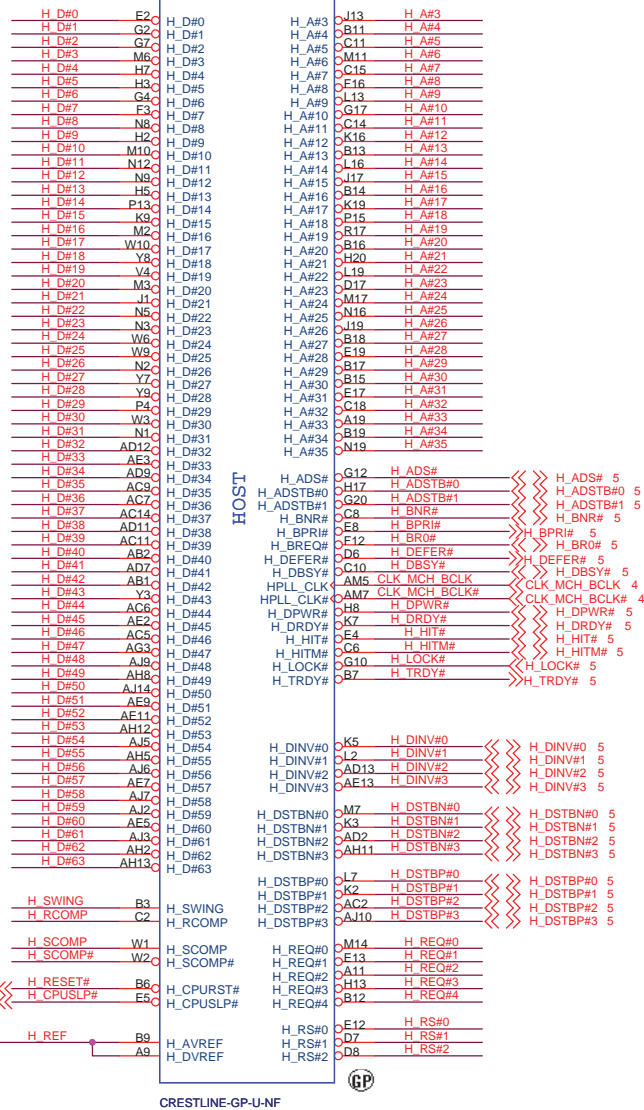
TPAD28 TP11 TEST3
 TPAD28 TP1 TEST5
 For the purpose of testability,
 route the signals through a ground
 referenced Zo=55ohm trace that ends
 in a via that is near a GND via
 and is accessible through an
 oscilloscope connection.

Make COMP[3..0] traces length shorter
 than 0.5". Trace should be at least 25
 mils away from any other toggling
 signal.
 COMP 0,2 connect Zo=27.4ohm.
 COMP 1,3 connect Zo=55ohm.

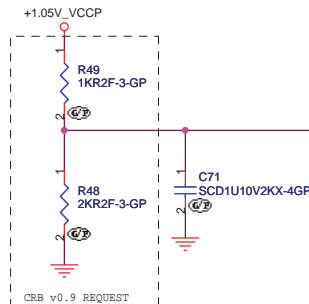


H_D#[63..0] <<>> H_D#[63..0] 5
H_A#[35..3] <<>> H_A#[35..3] 5
H_REQ#[4..0] <<>> H_REQ#[4..0] 5
H_RS#[2..0] >>> H_RS#[2..0] 5

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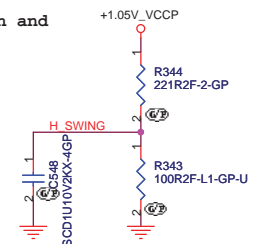
H_REF Decoupling Crestline
close Crestline 100 mil



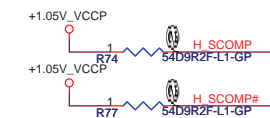
H_SWING routing Trace width and
Spacing use 10 / 20 mil

H_SWING Resistors and
Capacitors close
Caliistoga 500 mil (MAX)

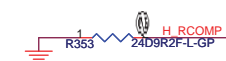
From Schematic Design
Checklit v.1201
221 1% pull high 100
1% pull low



H_SCOMP and H_SCOMP# Resistors
and Capacitors close Caliistoga
500 mil (MAX)
Zo=55ohms



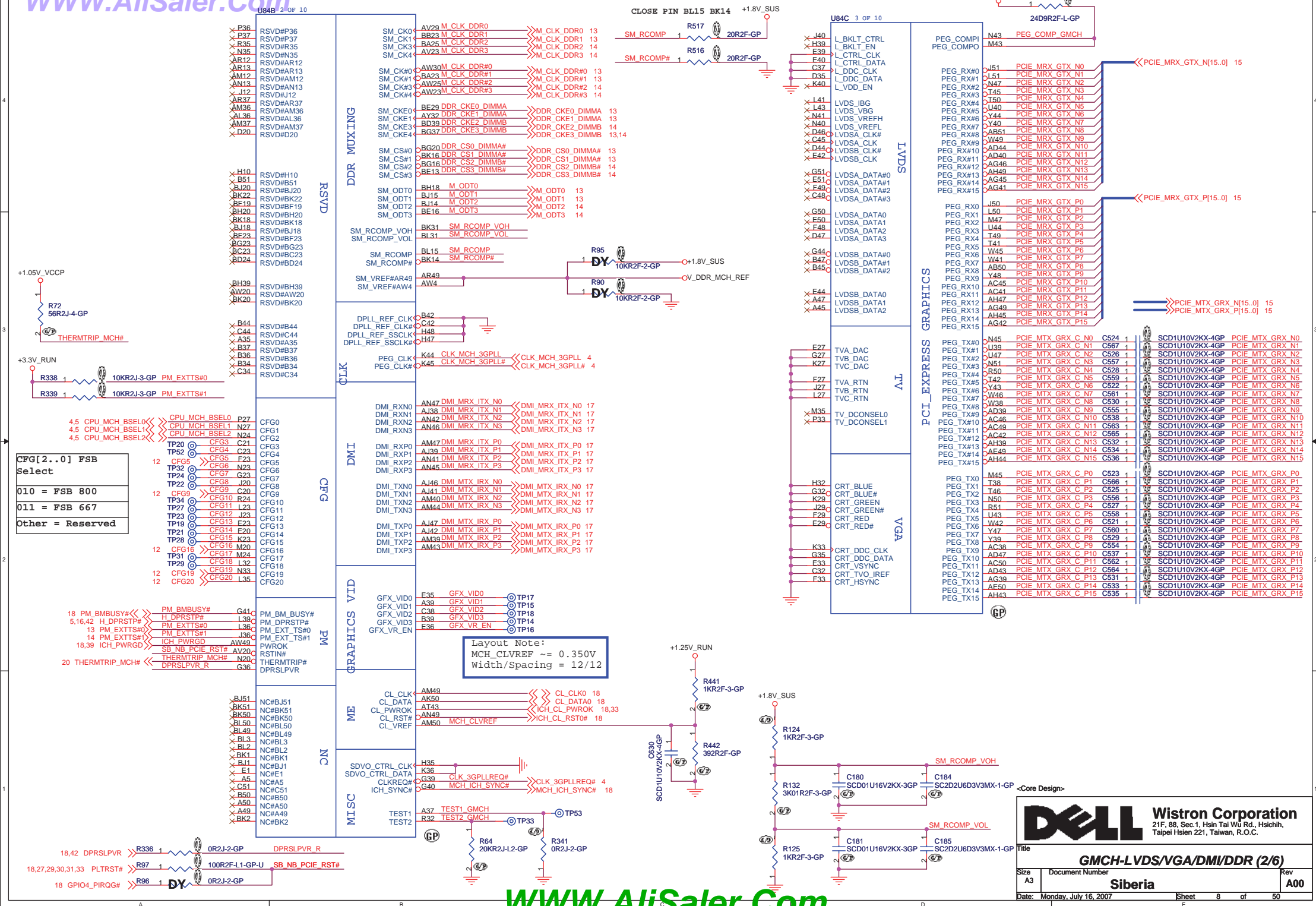
H_RCOMP routing Trace width and
Spacing use 10 / 20 mil

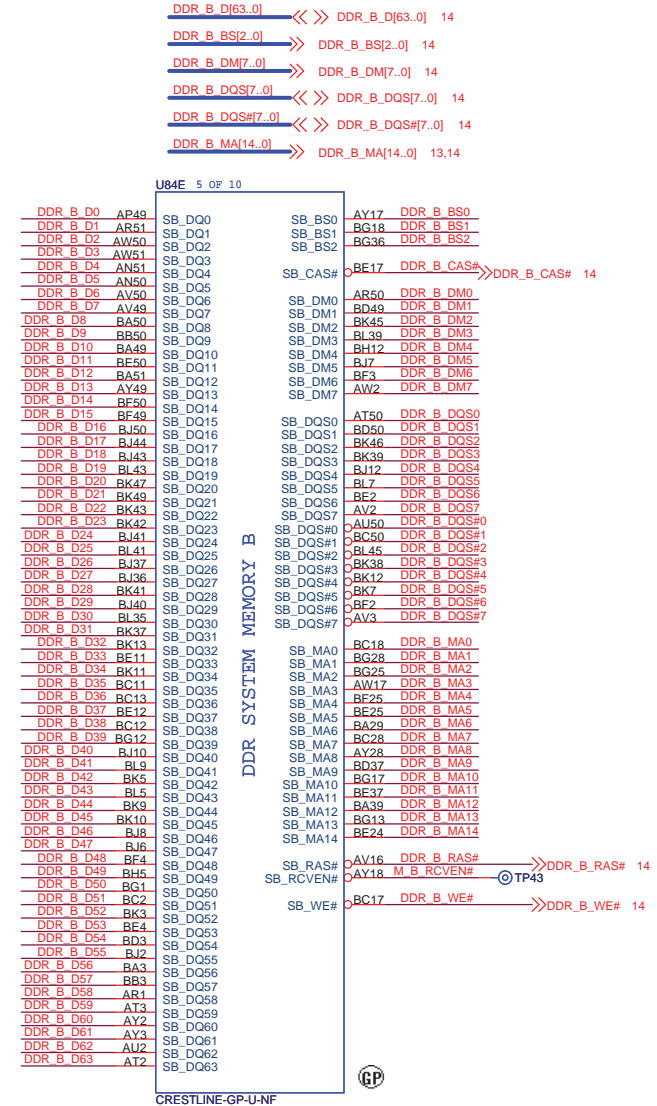
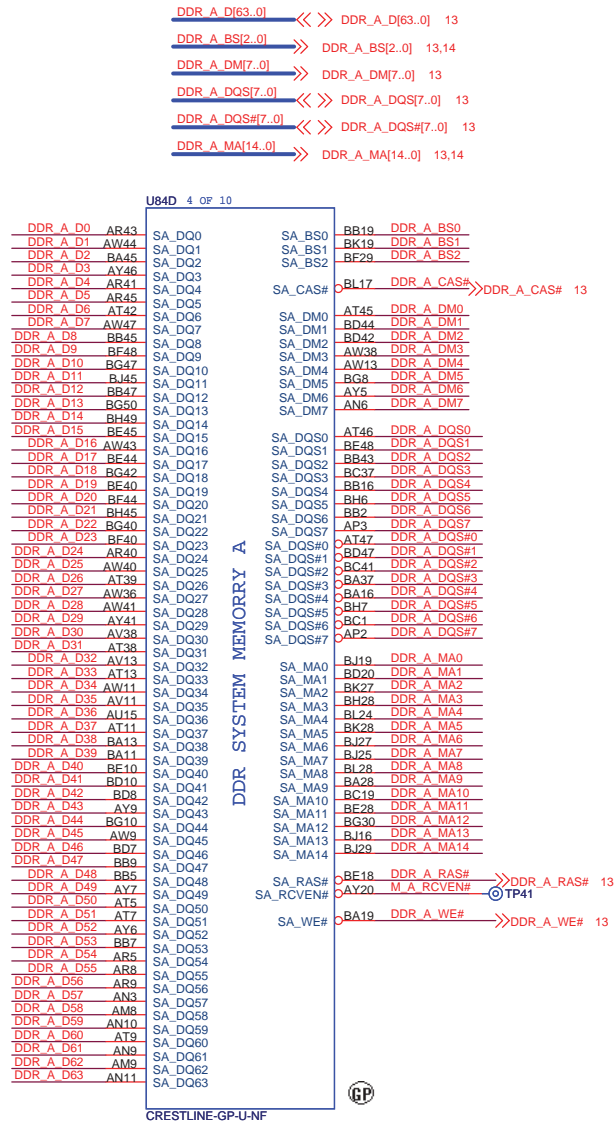


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Title: **GMCH-FSB LIBC (1/6)**
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VCC CORE 1.31A

POWER

VCC SM 2.4A

VCC GFX NCTF

VCC GFX

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

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VCC SM LF

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VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

VCC SM LF

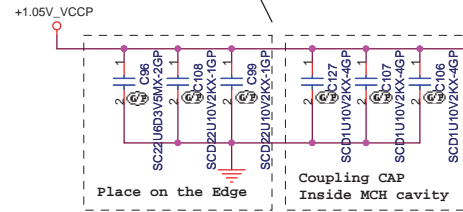
Supply	Signal Group	Icc-max
+1.05V_VCCP	VCC	1.31A
+1.05V_VCCP	VCC_NCTF	A
+1.05V_VCCP	VTT	0.85A
+1.05V_VCCP	VCC_PEG	1.2A
+1.05V_VCCP	VCC_RXR_DMI	0.25A
+1.05V_VCCP	VCC_ATX	84.15mA
+1.8V_SUS	VCC_SM	2.4A
+1.8V_SUS	VCC_SM_CK	0.2A
+1.25V_RUN	VCCA_HPLL	0.05A
+1.25V_RUN	VCCA_MPLL	0.15A
+1.25V_RUN	VCCA_SM	0.735A
+1.25V_RUN	VCCA_SM_NCTF	A
+1.25V_RUN	VCCA_SM_CK	0.015A
+1.25V_RUN	VCCD_HPLL	0.25A
+1.25V_RUN	VCCA_AXD	0.2A
+1.25V_RUN	VCCA_AXD_NCTF	A
+1.25V_RUN	VCCA_PEG_PLL	0.1A
+1.25V_RUN	/VCCD_PEG_PLL	0.35A
+1.25V_RUN	VCCA_AXF	0.1A
+1.25V_RUN	VCCA_DMI	0.1A
+1.5V_RUN	VCCD_TV DAC	0.06A
+3.3V_RUN	VCCA_PEG_BG	0.005A
+3.3V_RUN	VCC_HV	0.1A

(Non-AMT)

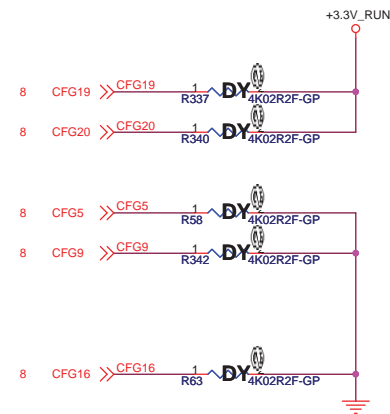
(667MHz)

(667MHz)

FOR VCC AXM NCTF AND VCC AXM

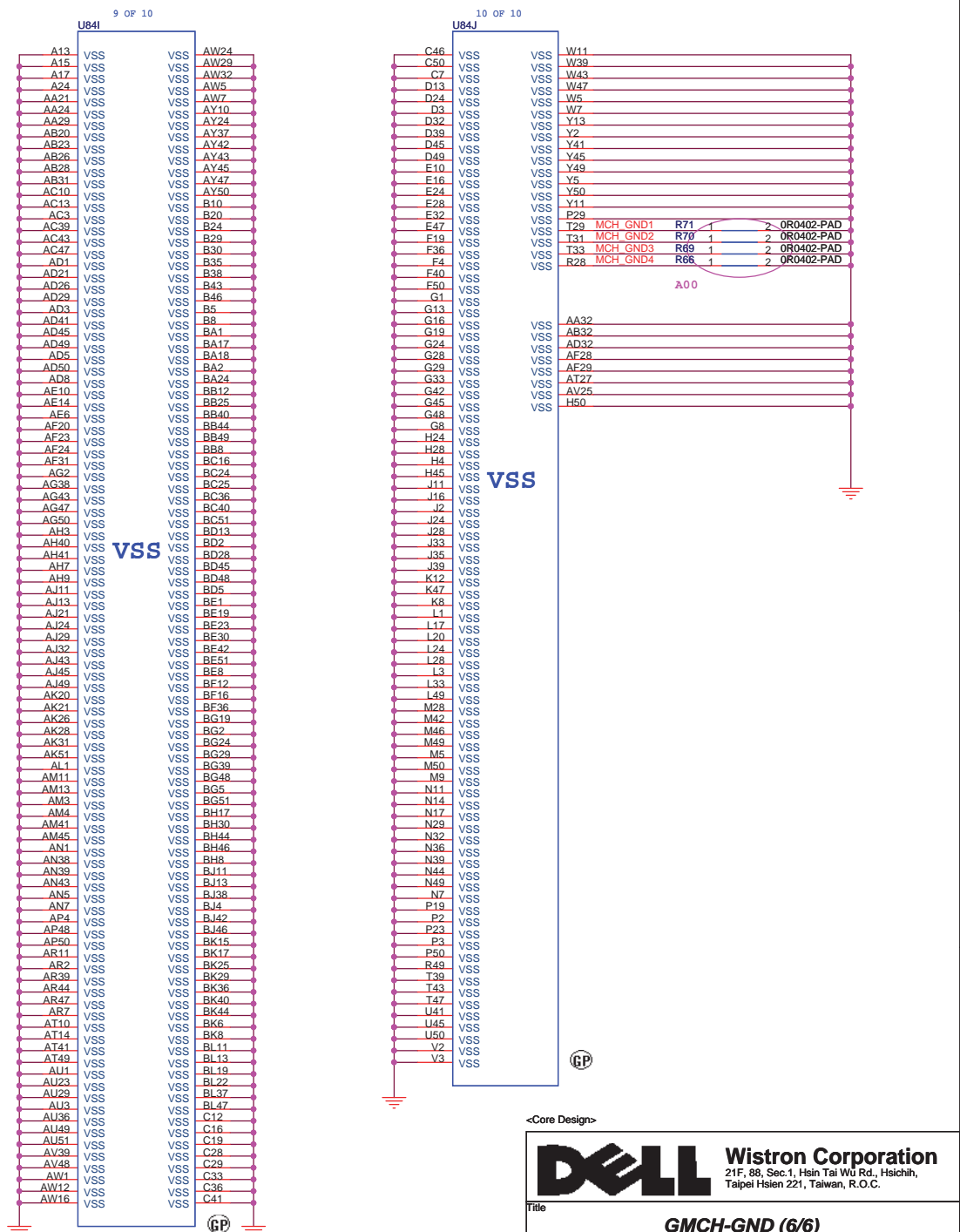


Layout Note:
Location of all MCH CFG strap resistors
need to be close to trace to minimize stub



CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)
CFG 16 FSB Dynamic ODT	Disabled	Enabled
CFG 18 VCC select	1.05V	1.5V
CFG 19 DMI Lane Reserved	Normal Operation	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation	PCIE and SDVO are operation simultaneous

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation



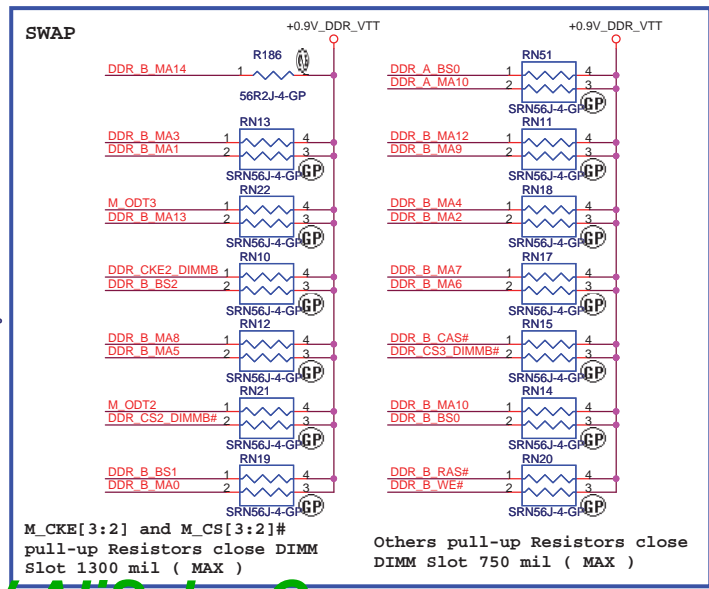
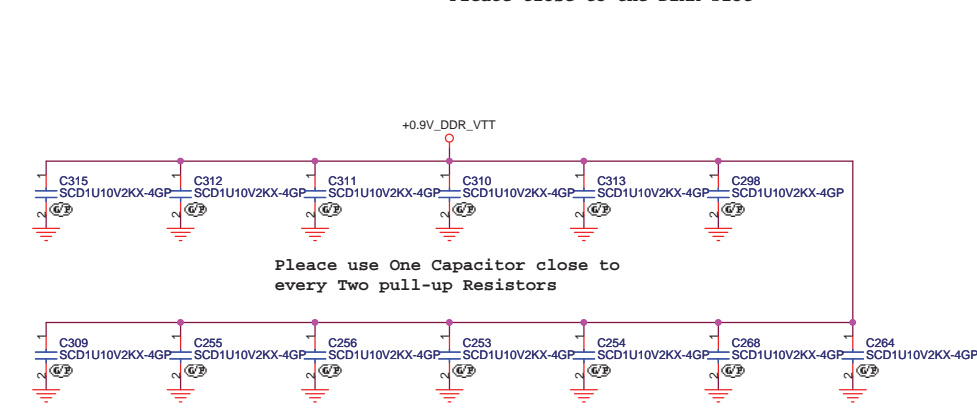
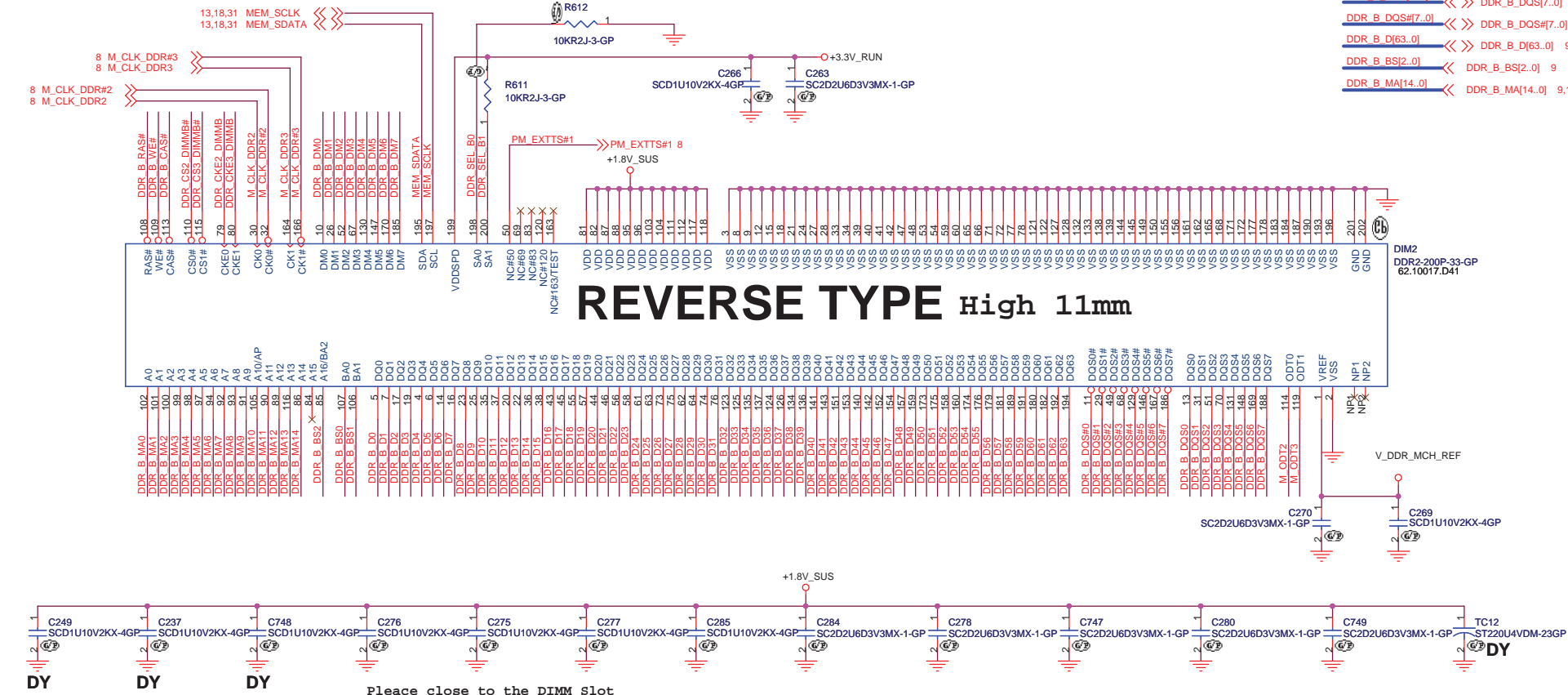
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Title: **GMCH-GND (6/6)**

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DDR_B_DM[7..0] << DDR_B_DM[7..0] 9
DDR_B_DQS[7..0] << DDR_B_DQS[7..0] 9
DDR_B_DQS#7..0 << DDR_B_DQS#7..0 9
DDR_B_D[63..0] << DDR_B_D[63..0] 9
DDR_B_BS[2..0] << DDR_B_BS[2..0] 9
DDR_B_MA[14..0] << DDR_B_MA[14..0] 9,13

DIM2
DDR2-200P-33-GP
62.10017.D41

V_DDR_MCH_REF

C270 SC2D2U6D3V3MX-1-GP
C269 SCD1U10V2KX-4GP

TC12 ST220U4VDM-23GP
DY

Place close to the DIMM Slot

SWAP

+0.9V_VTT

DDR_B_MA14
DDR_B_MA3
DDR_B_MA1
M_ODT3
DDR_B_MA13
DDR_CKE2_DIMMB
DDR_B_BS2
DDR_B_MA8
DDR_B_MA5
M_ODT2
DDR_CS2_DIMMB#
DDR_B_BS1
DDR_B_MA0

DDR_A_BS0
DDR_A_MA10
DDR_B_MA12
DDR_B_MA9
DDR_B_MA4
DDR_B_MA2
DDR_B_MA7
DDR_B_MA6
DDR_B_MA10
DDR_B_BS0
DDR_B_RAS#
DDR_B_WE#

DDR_A_BS0 << DDR_A_BS0 9,13
DDR_A_MA10 << DDR_A_MA10 9,13

DDR_CS2_DIMMB# << DDR_CS2_DIMMB# 8
DDR_CS3_DIMMB# << DDR_CS3_DIMMB# 8
DDR_CKE2_DIMMB << DDR_CKE2_DIMMB 8
DDR_CKE3_DIMMB << DDR_CKE3_DIMMB 8,13
DDR_B_RAS# << DDR_B_RAS# 9
DDR_B_CAS# << DDR_B_CAS# 9
DDR_B_WE# << DDR_B_WE# 9
M_ODT2 << M_ODT2 8
M_ODT3 << M_ODT3 8

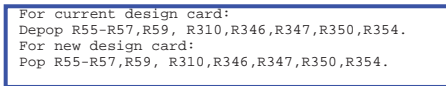
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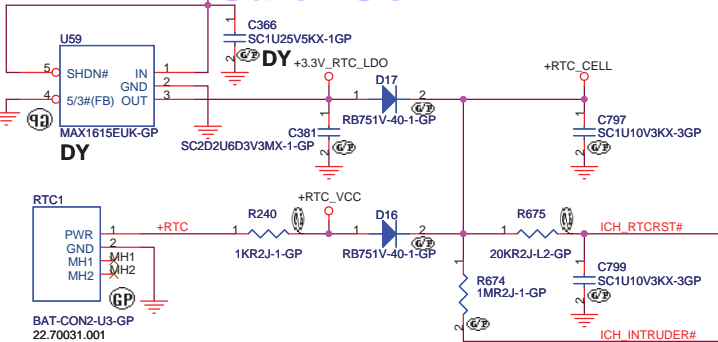
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Title
DDR2-SODIMM2

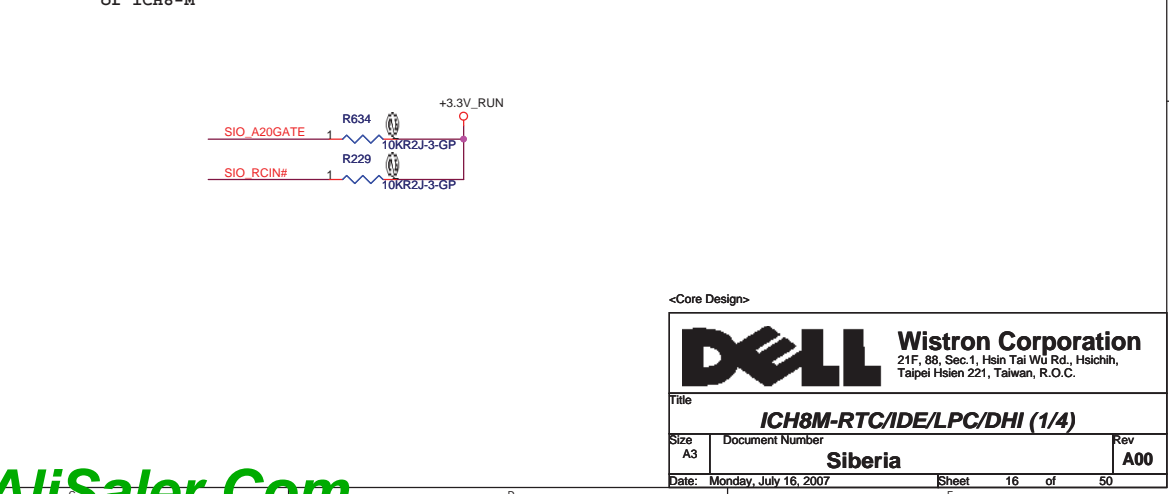
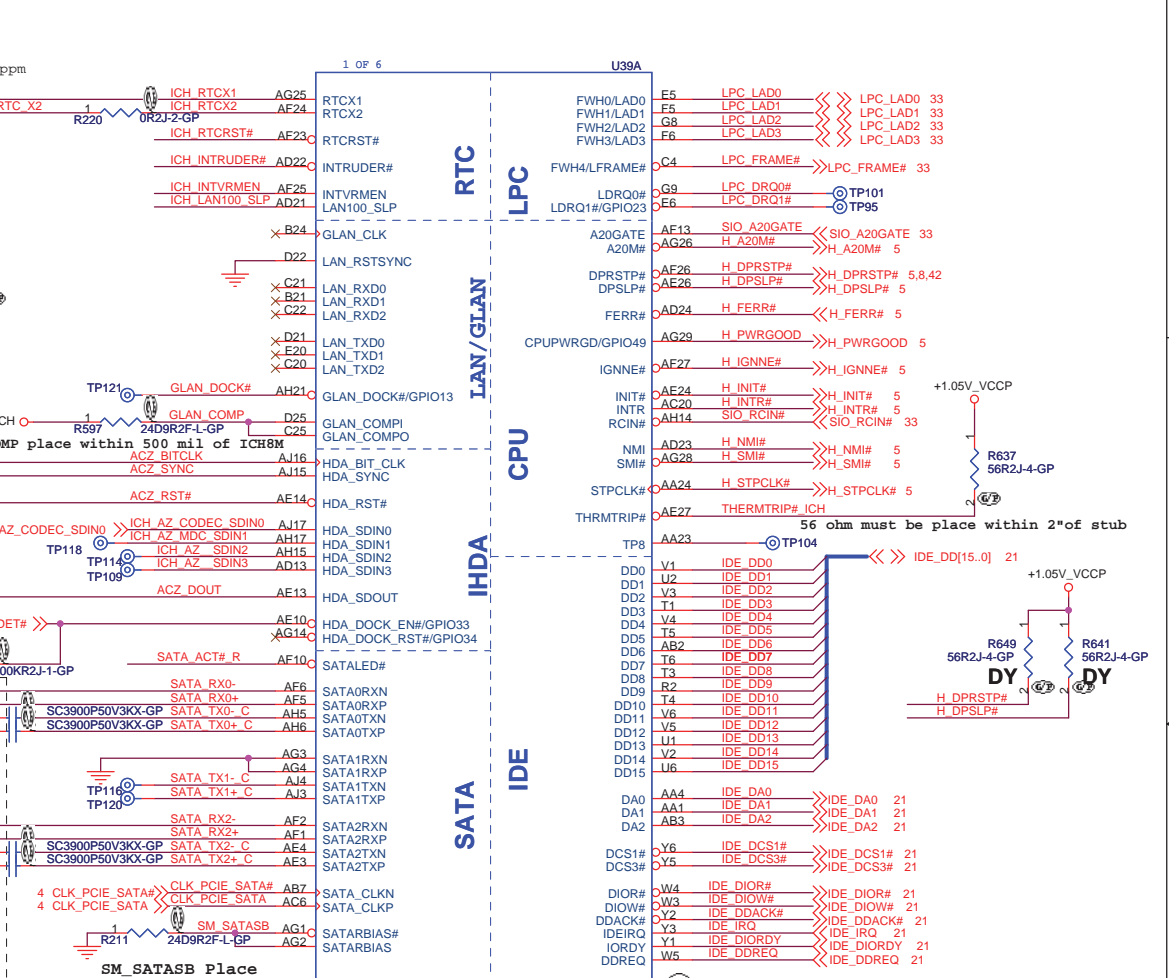
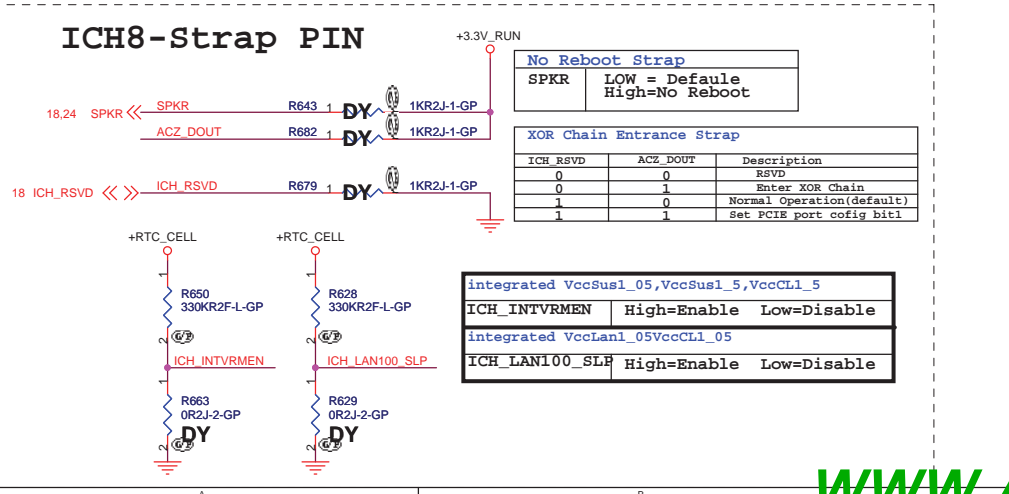
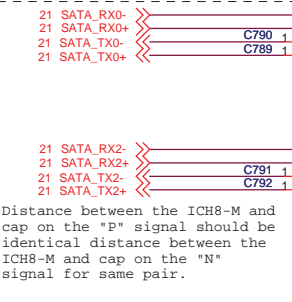
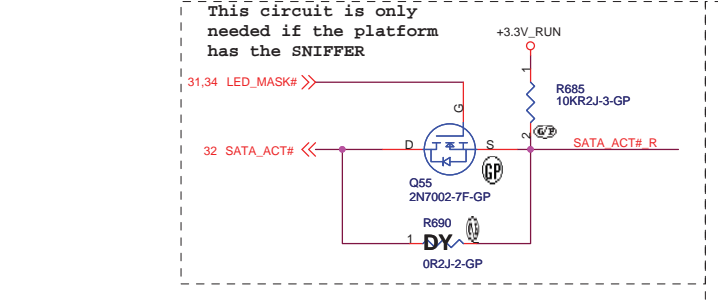
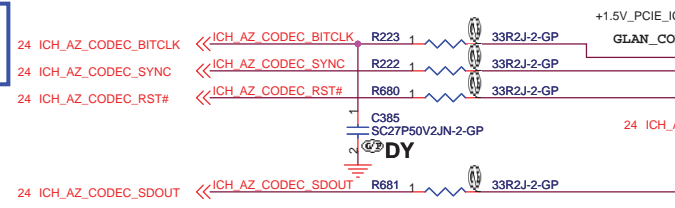
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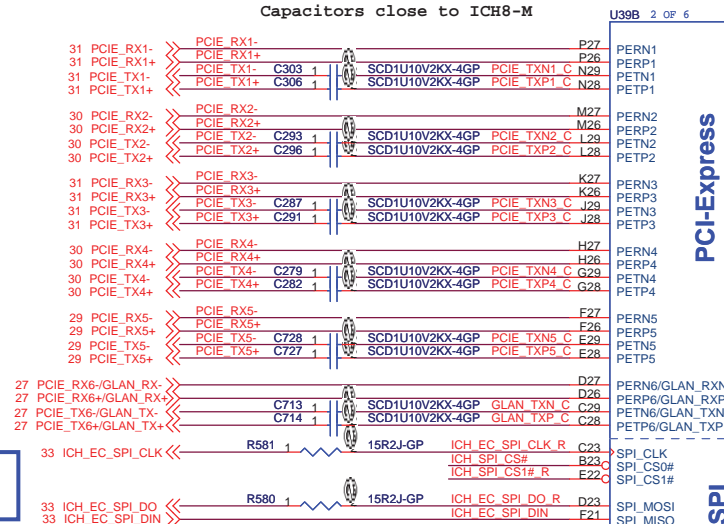
Place all series terms close to ICH8 except for SDIN input lines, which should be close to source.



PCIE Interface Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	MiniCard WPAN
LANE4	Express Card
LANE5	PPU Card
LANE6	Giba Bit LOM

PCIE TX dc blocking Capacitors close to ICH8-M



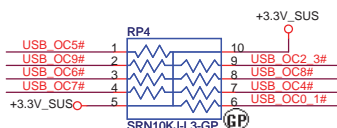
Layout Note:
Place R563, R580 and R581
within 500 mils from ICH.

ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R617)	SPI_CS#1 (R623)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R620)	low = A16 swap override enable high = default	



USB OC# PULL HIGH



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PCI-Express

Direct Media Interface

SPI

USB

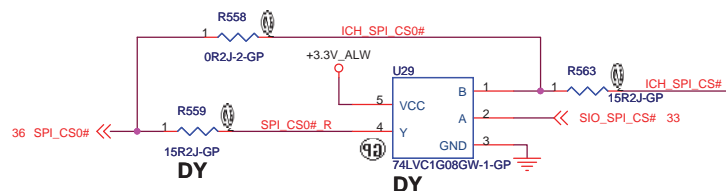


DMI_COMP R622 place
within 500 mil of ICH8M

ICH

USB0	Ext Left Side
USB1	Ext Back
USB2	Ext Right Side (Top)
USB3	Ext Right Side (Bottom)
USB4	3rd mini card
USB5	Camera
USB6	Express Card
USB7	BT
USB8	Gaming LCD
USB9	WWAN

USBRBIAS close to ICH8M 500
mils and Trace impedance
should be 60 ohm +/- 15%



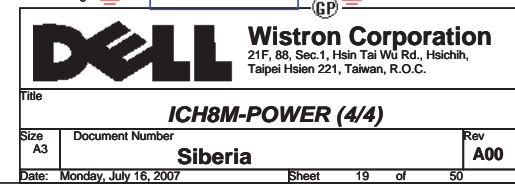
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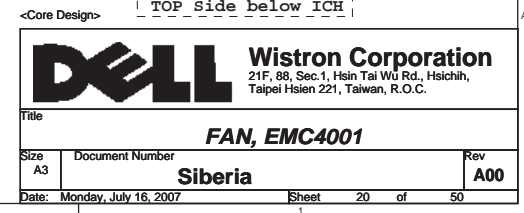


Title		
ICH8M-PCIE/USB/SPI/DMI (2/4)		
Size	Document Number	Rev
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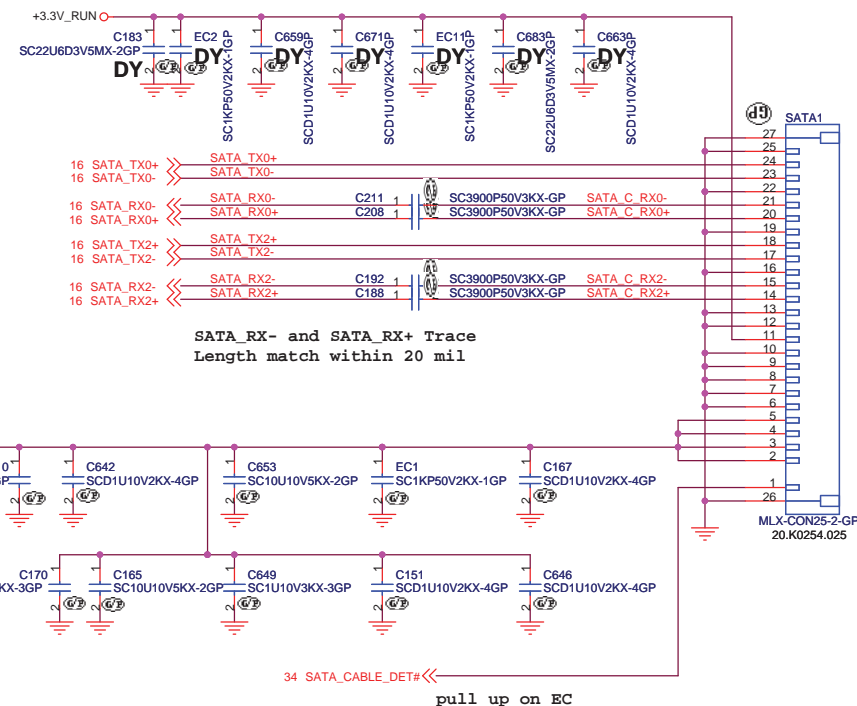
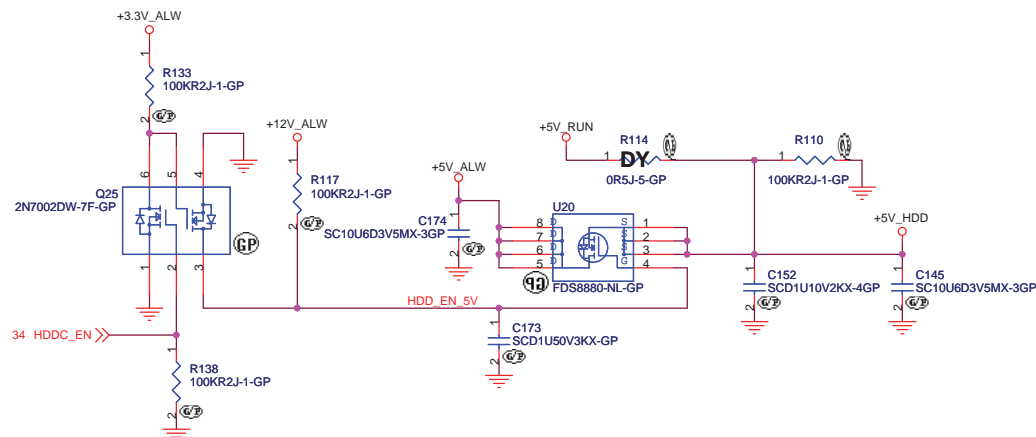

```
PCI_REQ#0  ────┐
                │
                └───>> PCI_GNT#0  17
                └───>> PCI_GNT#1  28
```



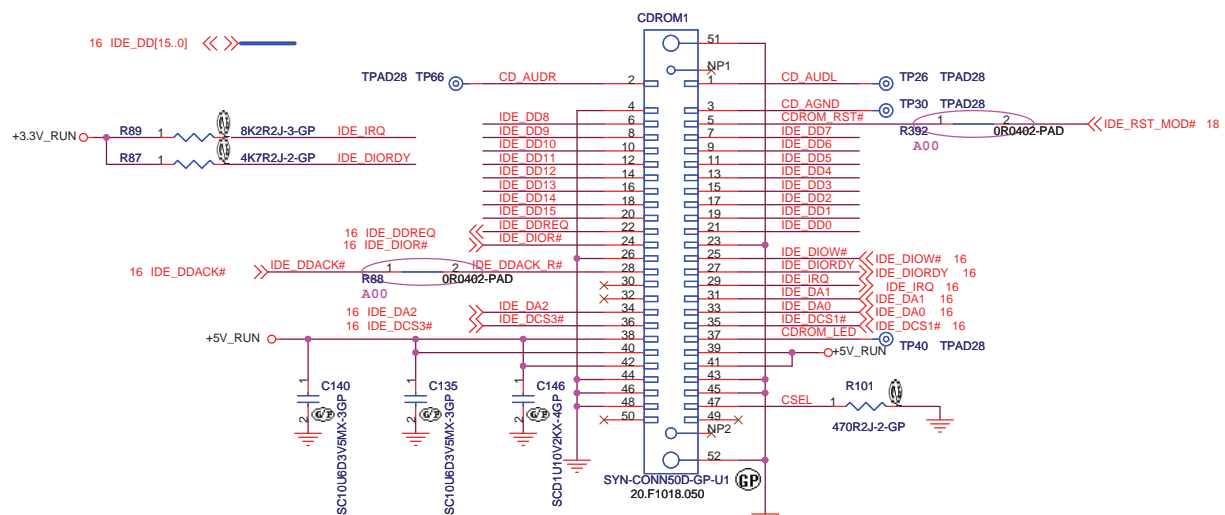


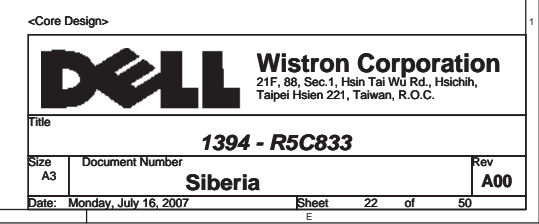


SATA HDD Connector

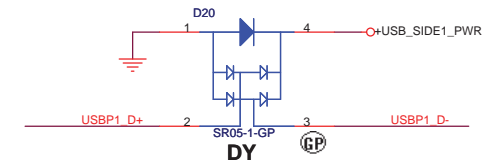
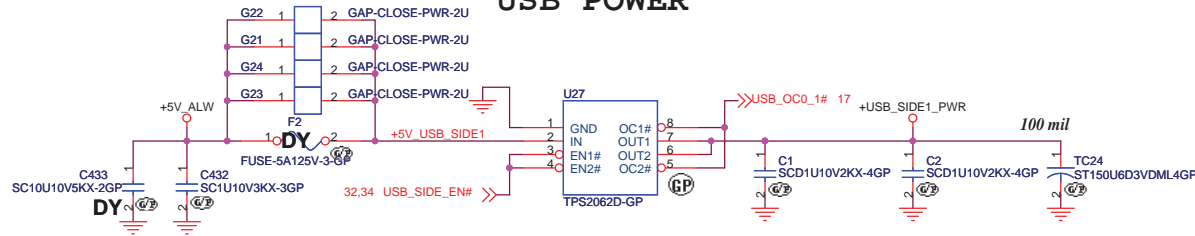


ODD Connector

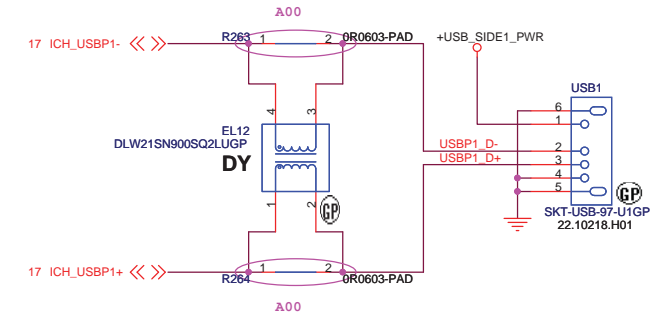




USB POWER

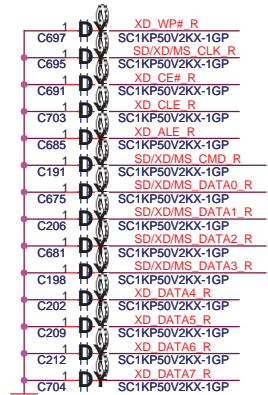
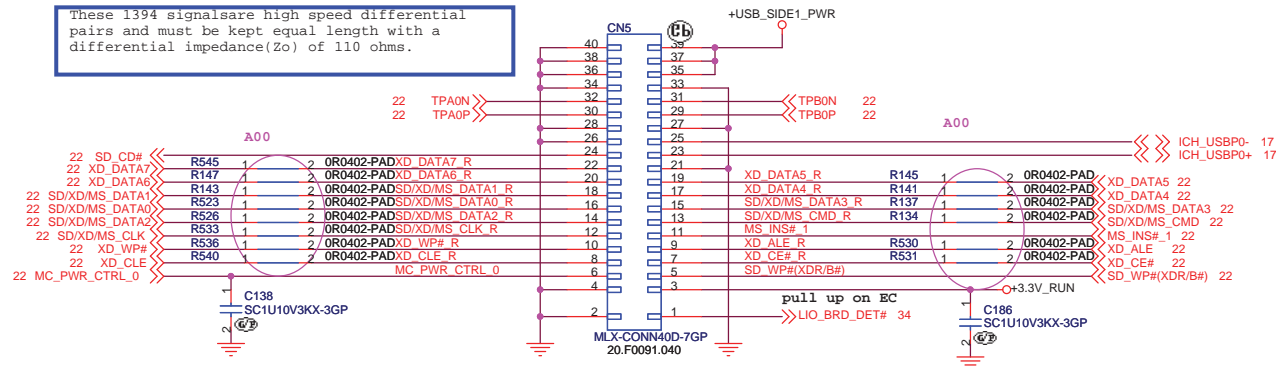


Place ESD diodes as close to the connector as possible.



I/O board conn. (1394/7 IN 1/USB)

These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Z_0) of 110 ohms.

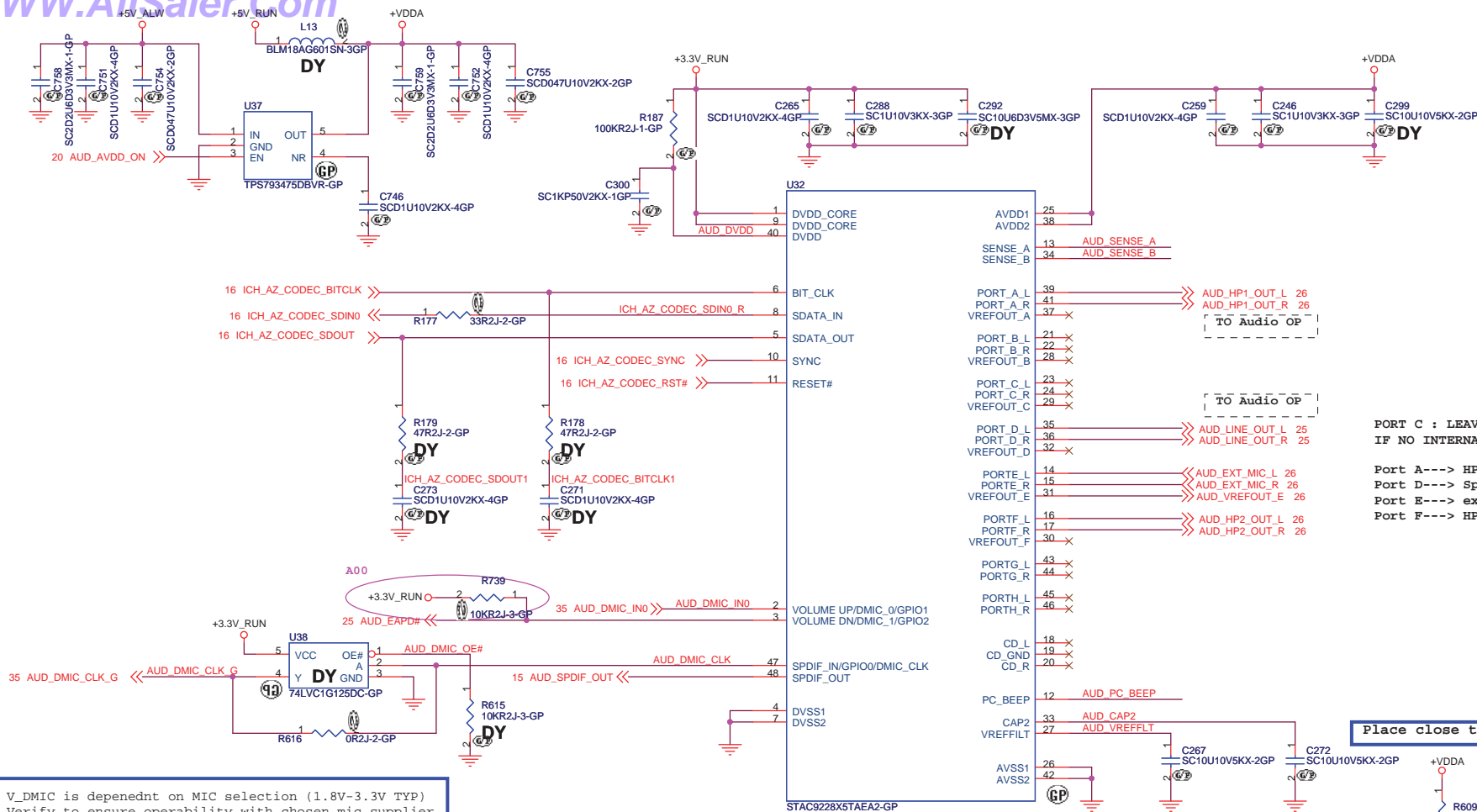


<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: I/O board (1394/7 IN 1/USB) / USB CONN.

Size: A3 Document Number: Siberia Rev: A00
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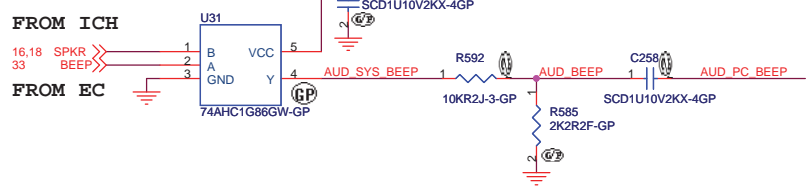
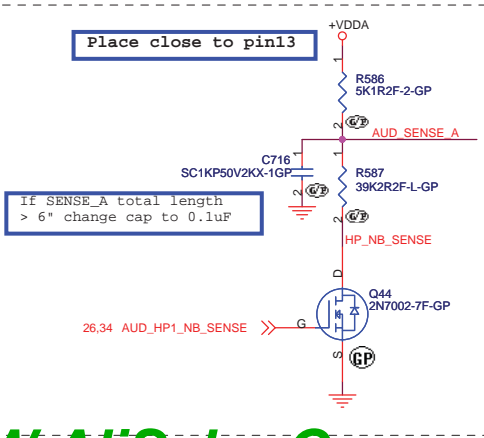
V_DMIC is dependednt on MIC selection (1.8V-3.3V TYP)
Verify to ensure operability with chosen mic supplier.
Note1: If only 1 digital mic, use AUD_DMIC_IN0.
Note2: If using 2 digital mics, also use AUD_DMIC_IN0.
This input supports 2 digital mics.
AUD_DMIC_IN1 is only used to support 4 digital mics.

PORT C : LEAVE NC
IF NO INTERNAL MICS.

Port A----> HP1
Port D----> Speaker
Port E----> ext Mic
Port F----> HP2

Place close to pin34

If SENSE_B total length
> 6" change cap to 0.1uF



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO (1/3)**

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Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.

Place filters close to the power pins - 47pF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.

Place one cap close to each of the pins, 38, 45 and 52.

Place resistor as close as possible to the ASIC. Pad is needed to measure 125MHz clock for debugging.

Important Layout Note for Dual footprint design:
Atmel part is available in standard package size, where as ST-Micro part is available in narrow package size. Ensure that pads are laid out for both footprint.
Recommendation: Pads for pins 1 (reference) through 4 can be standard and identically located for both packages. Pads for pins 5-8 need to be larger to accommodate both packages.

LOM_CABLE_DETECT goes to an input on a system microcontroller that can poll this signal periodically and can de-assert the LOM_LOM_PWR when LOM_CABLE_DETECT signal is high. Connect to an EC GPIO defined by th GPIO mapping.

Layout Note:
PNP Q3 and Q64 needs 0.5 inch by 0.5 inch thermal relief pad.

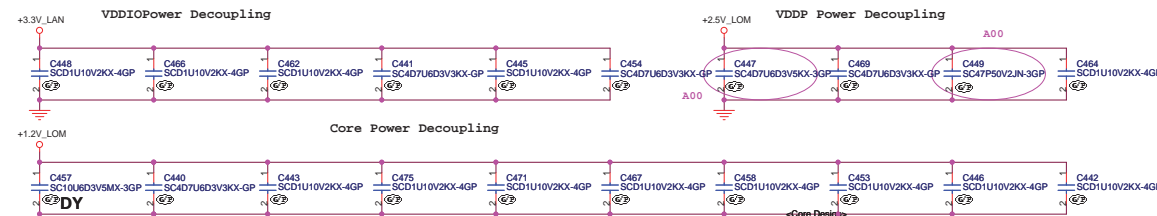
REGSEN12 and REGSEN25 should be routed using a trace from the load (PNP) back to the controller. Do not use a direct connection to the power plane.
Use 8mils trace width for these signals

Place C477 as close to pin17 of LOM as possible.

Place C457 as close to pin13 of LOM as possible.

Place high-frequency decoupling cpas close to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.

	SO	SI	CS#	SCLK
Ato-Sense Mode	0	0	1	0
ST M45PE10	1	0	0	0
Atmel AT45DB011B	1	1	0	0

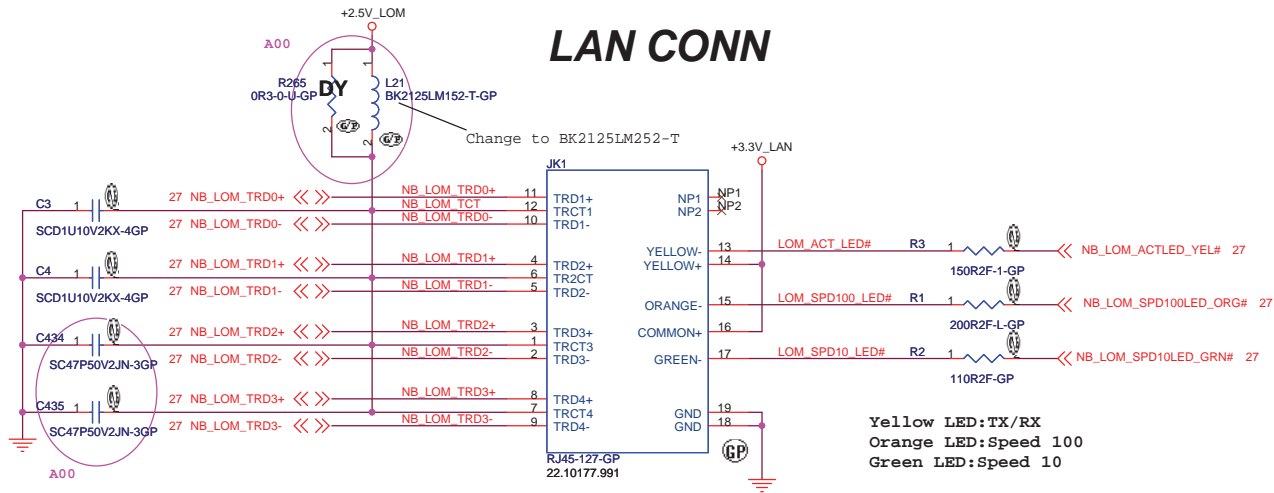


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File: **LAN BCM5754M**

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1. Route as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. Pairs must be equal lengths.
5. 4mil trace width,7mil separation.
6. 30mil between pairs and any other trace.
7. Must not cross ground moat,except RJ-45 moat.

The blowout from the LAN magnetics to the RJ45 connector maintaining the distance between the two to be within 1 inch.

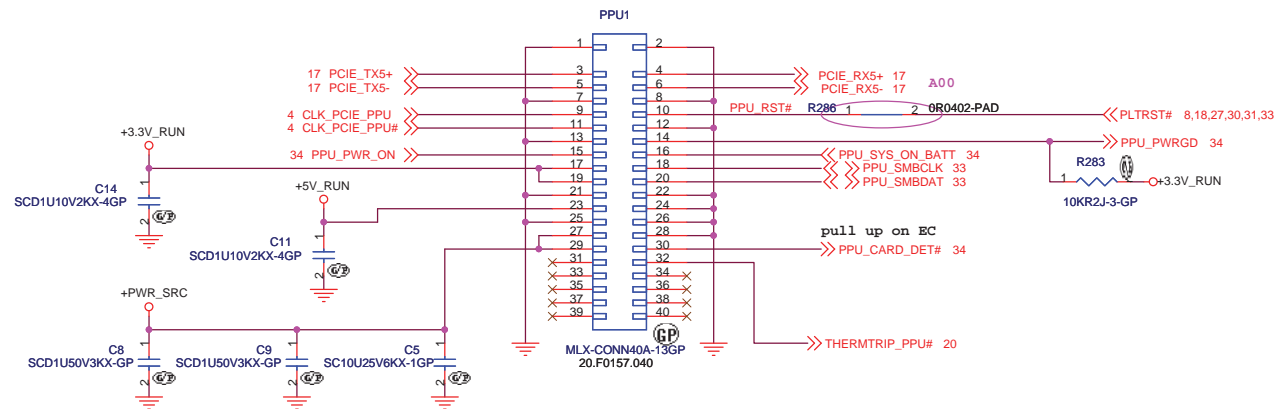
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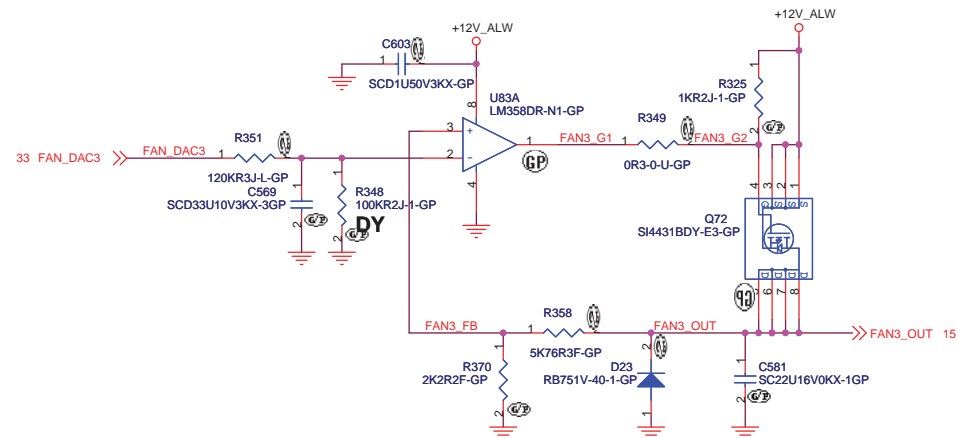
Title: **LAN Connector**

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PPU connector



2nd GPU FAN



<Core Design>



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	Title
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PPU CONN. / 2rd GPU FANSize
A3

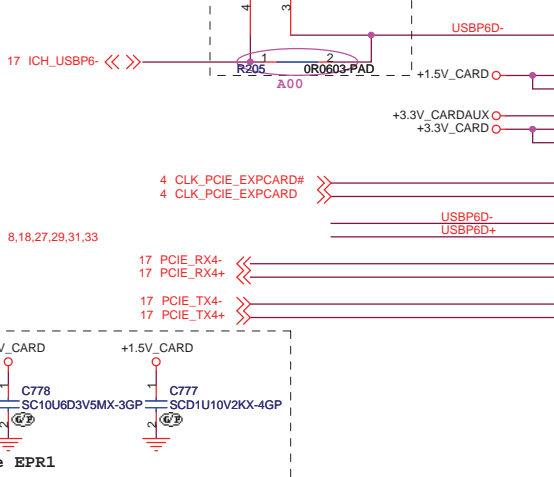
Document Number

Siberia

Rev	
A00	

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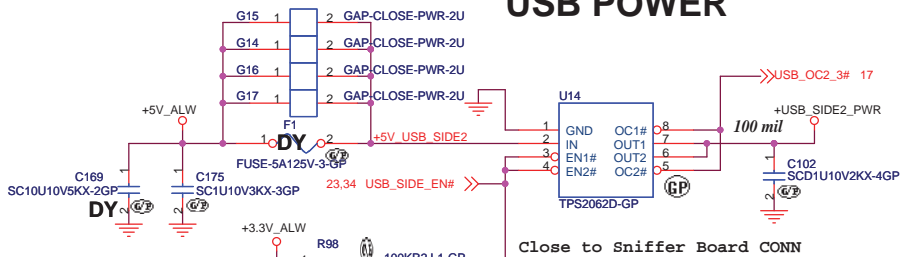
The schematic diagram illustrates the electrical connections for the USB card reader. A +3.3V_RUN supply is connected to the VCC pin of an RN42 SRN100KJ-6-GP resistor. The other end of the resistor is connected to a common ground line. This ground line is also connected to the GND pins of two connectors: one for PCIE_MCARD1_DET# and another for USB_MCARD1_DET#. A +1.5V_RUN supply is also shown connected to the common ground line.

MINICARD1

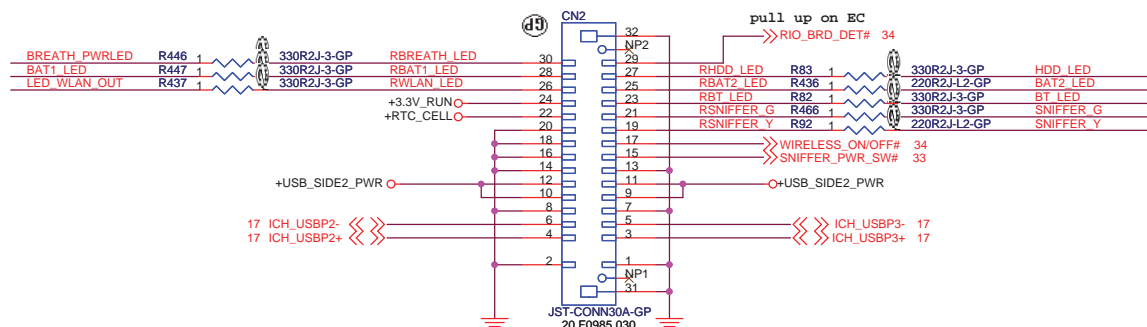




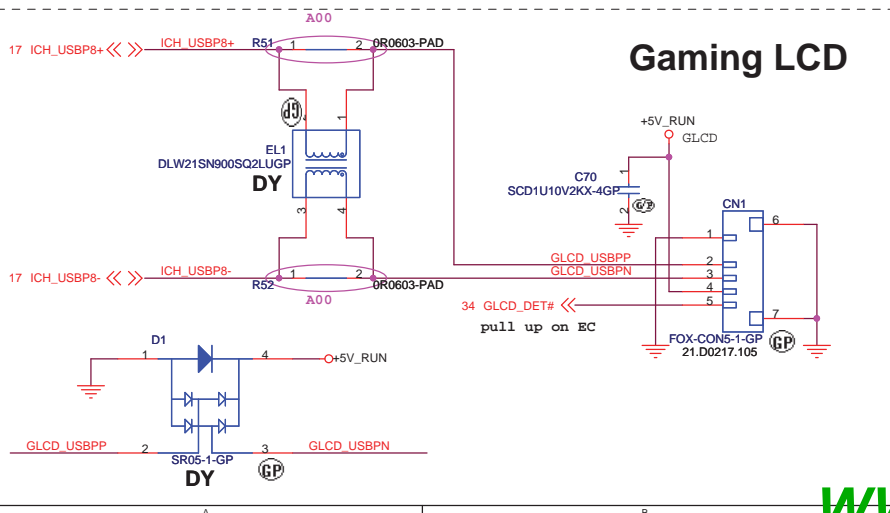
USB POWER



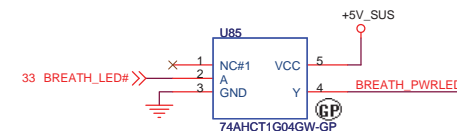
Sniffer board for USB, Indicator LEDs, Sniffer Switch conn.



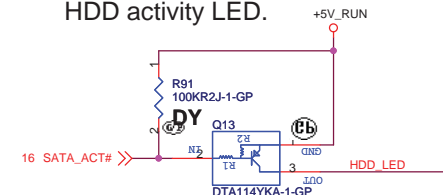
Gaming LCD



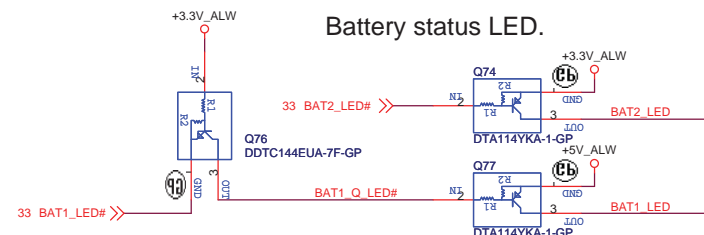
Power & Suspend LED.



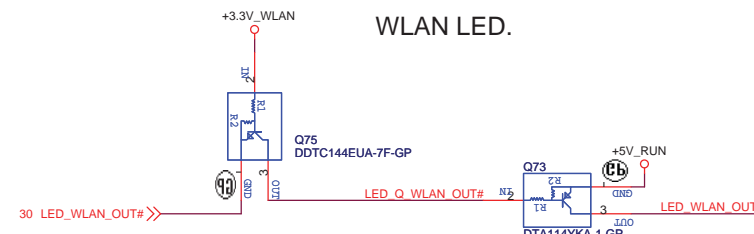
HDD activity LED.



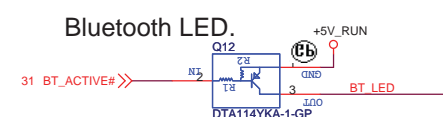
Battery status LED.



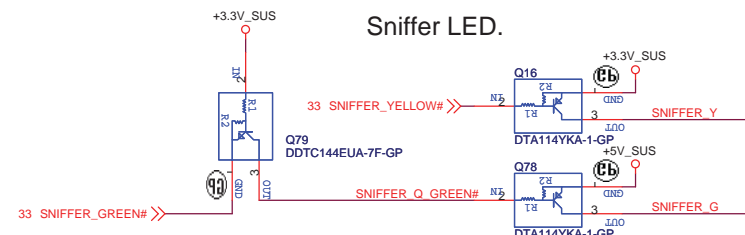
WLAN LED.



Bluetooth LED.



Sniffer LED.



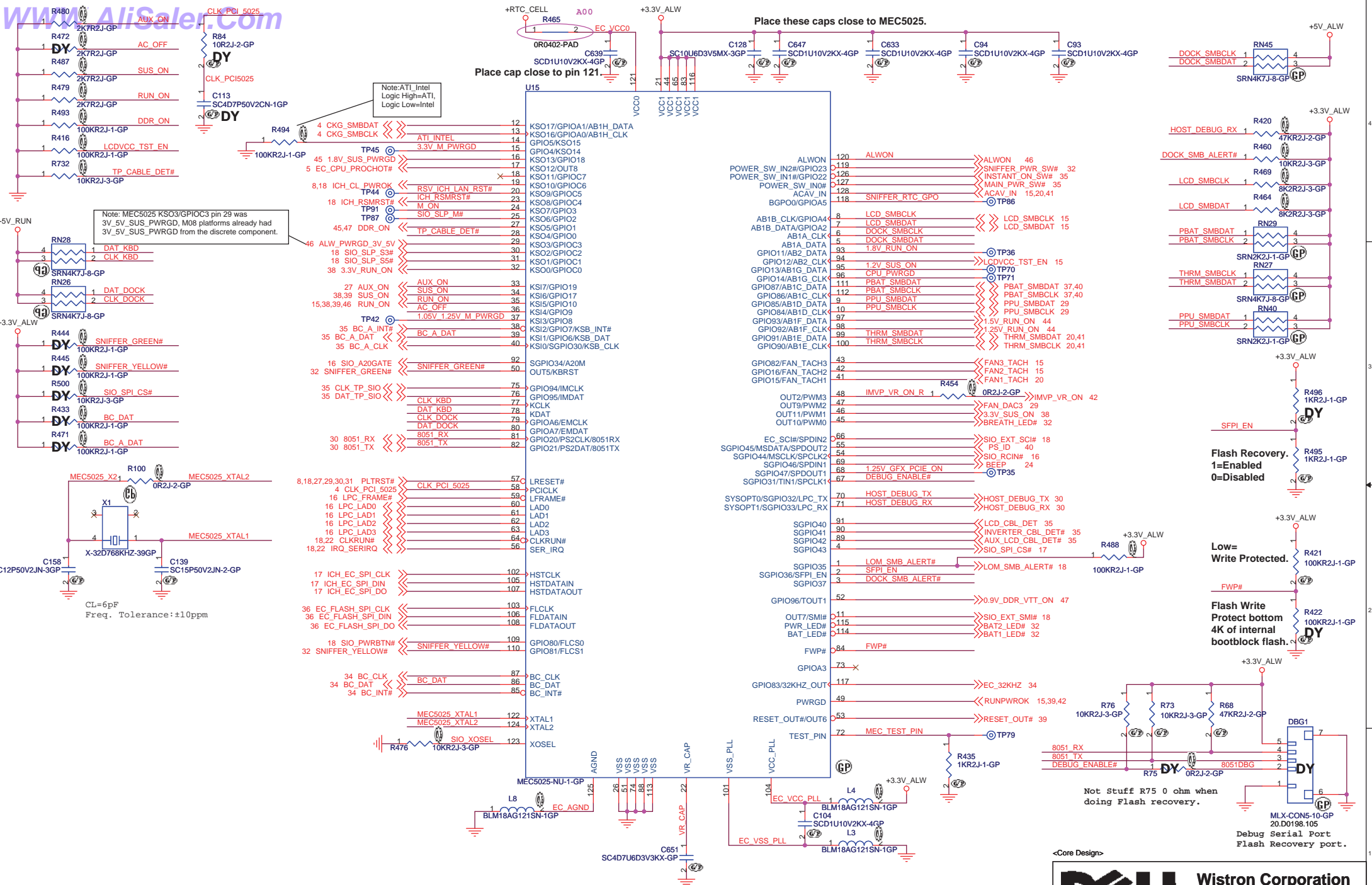
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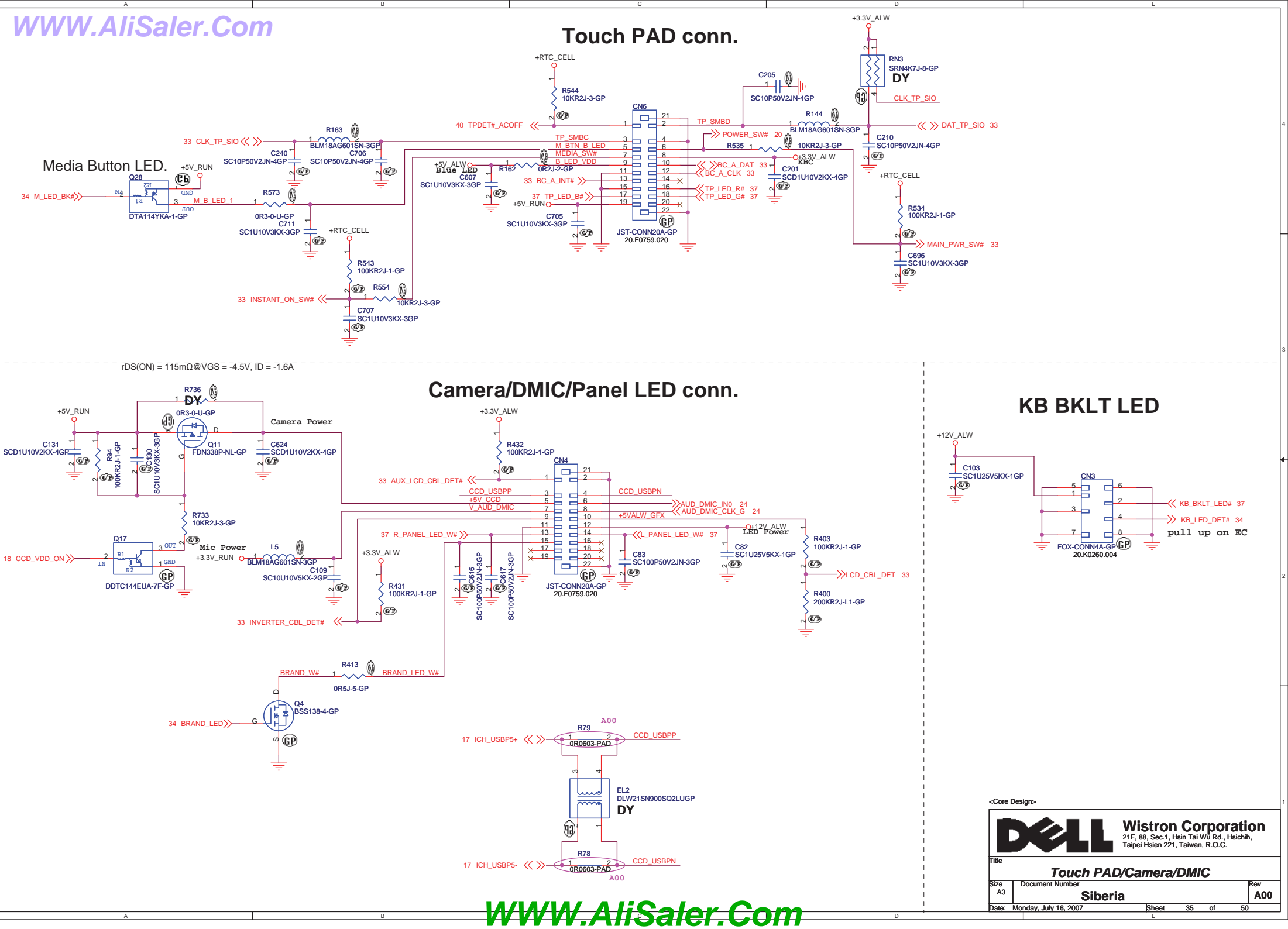
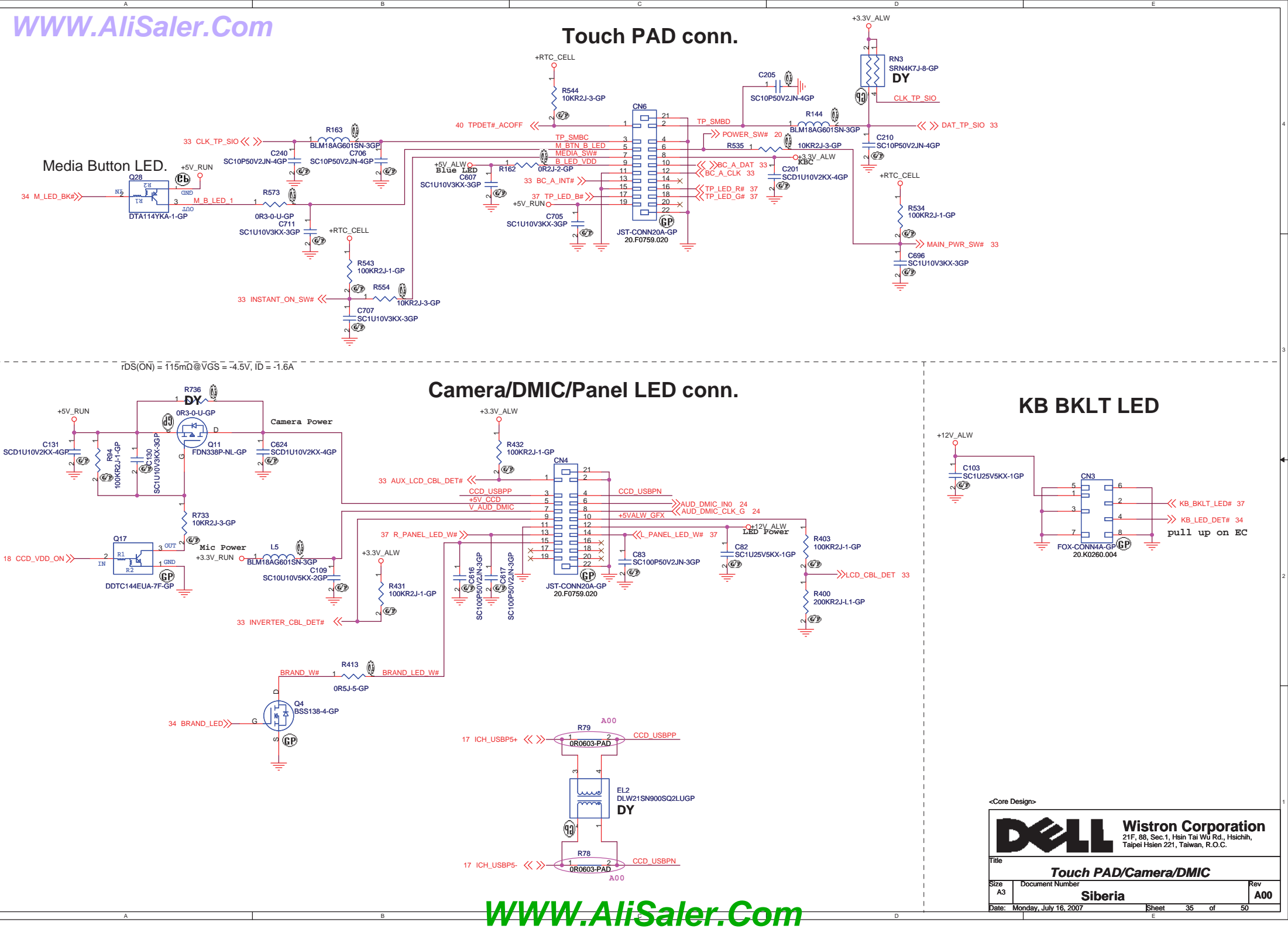
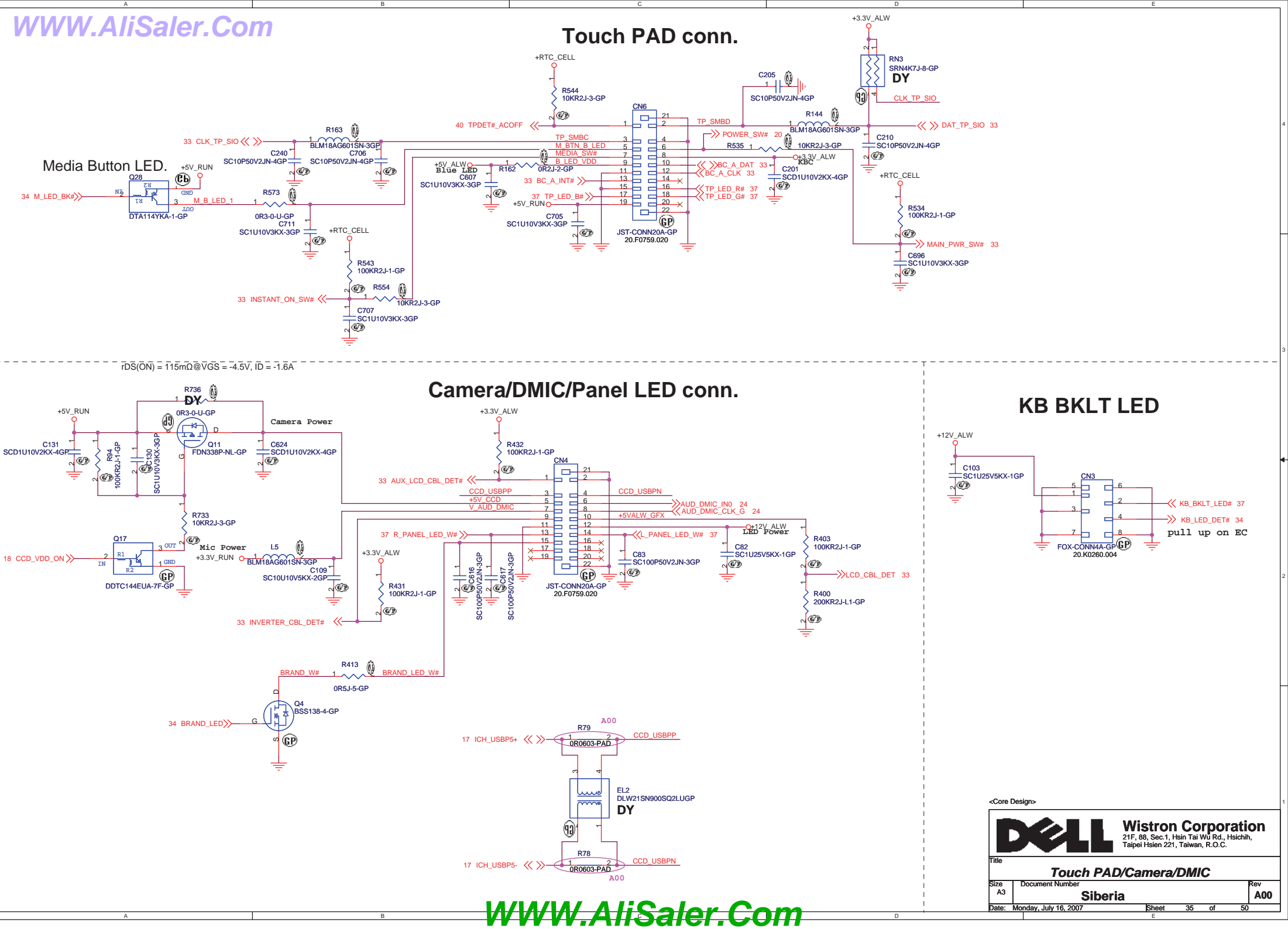
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Sniffer board (USB/Status LEDs) / Gaming LCD**

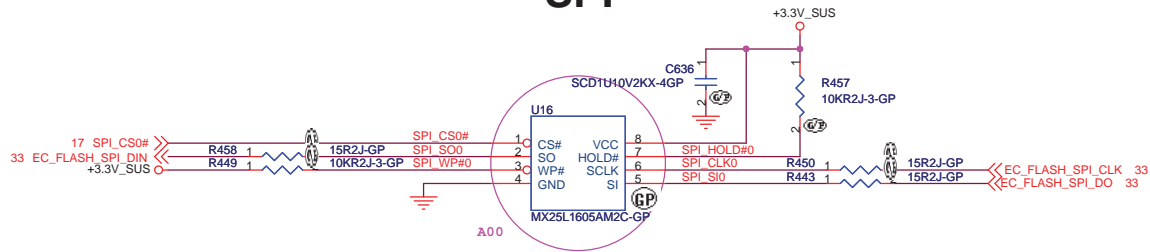
Size: A3 Document Number: **Siberia** Rev: **A00**

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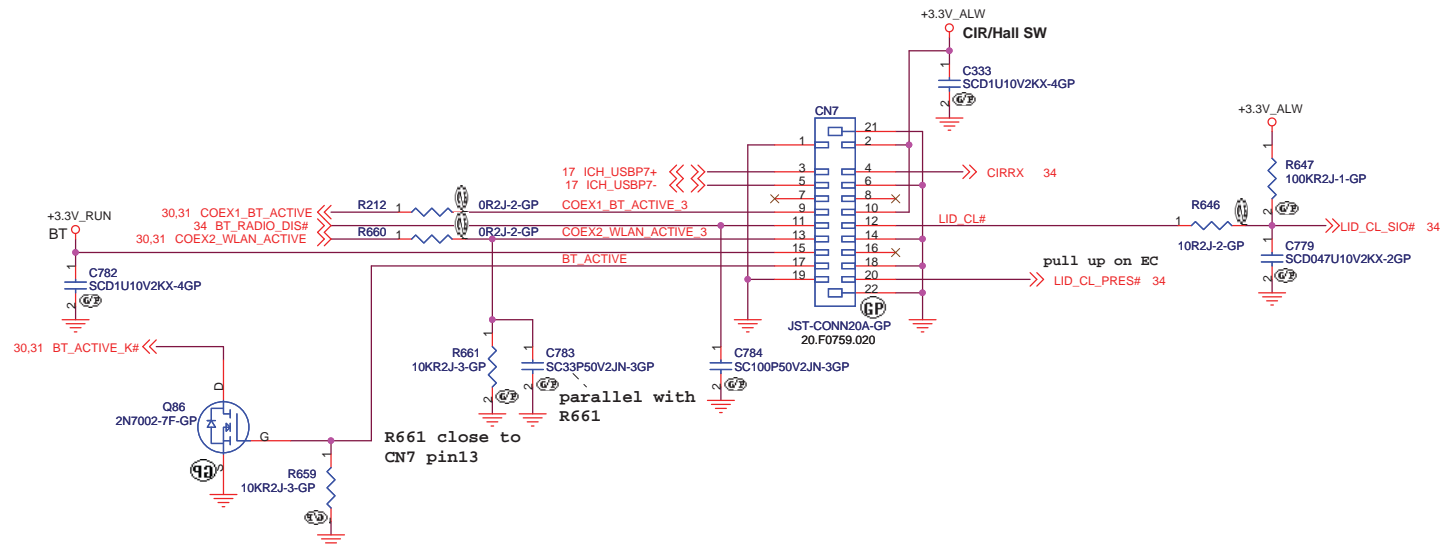


[illegible][illegible][illegible]

SPI



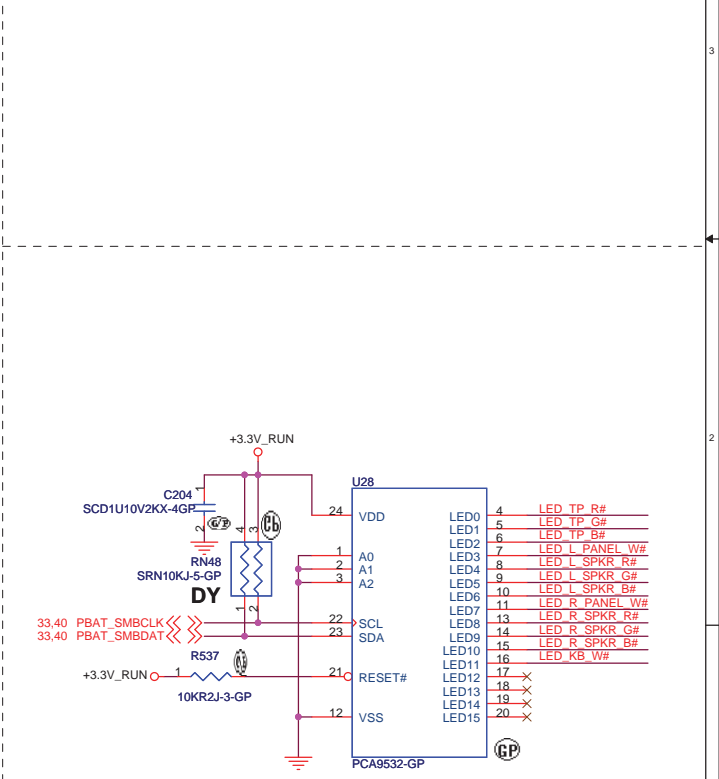
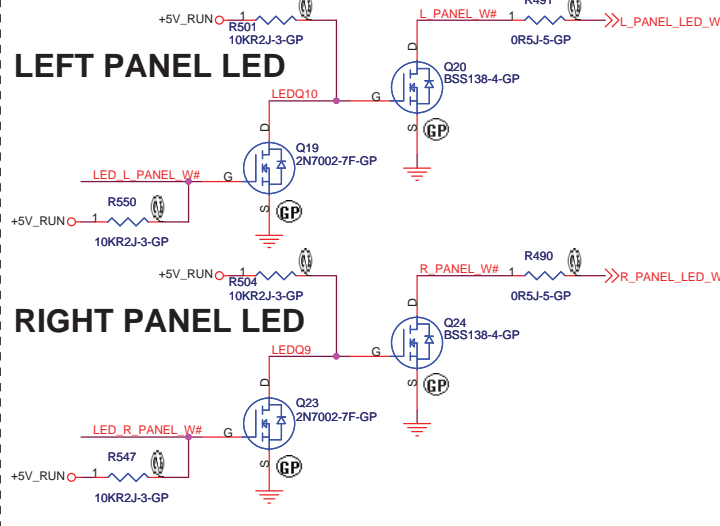
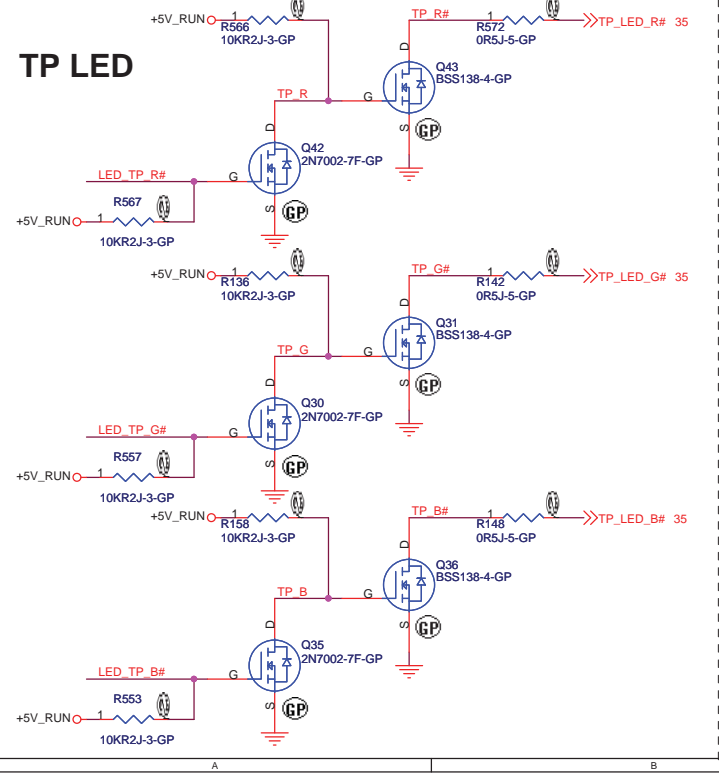
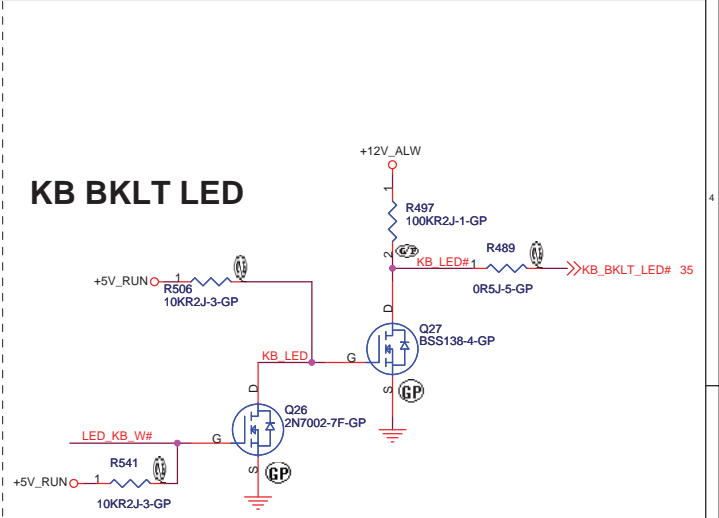
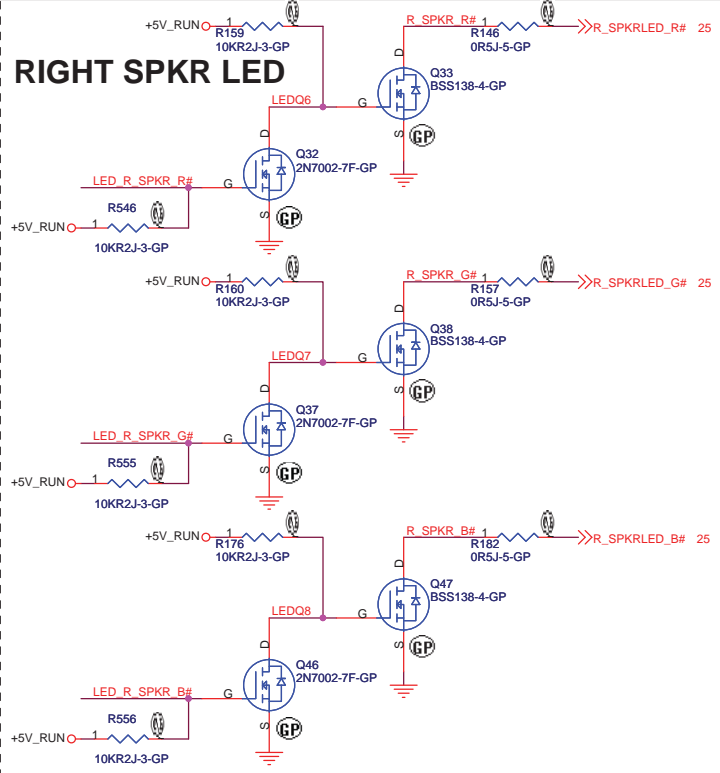
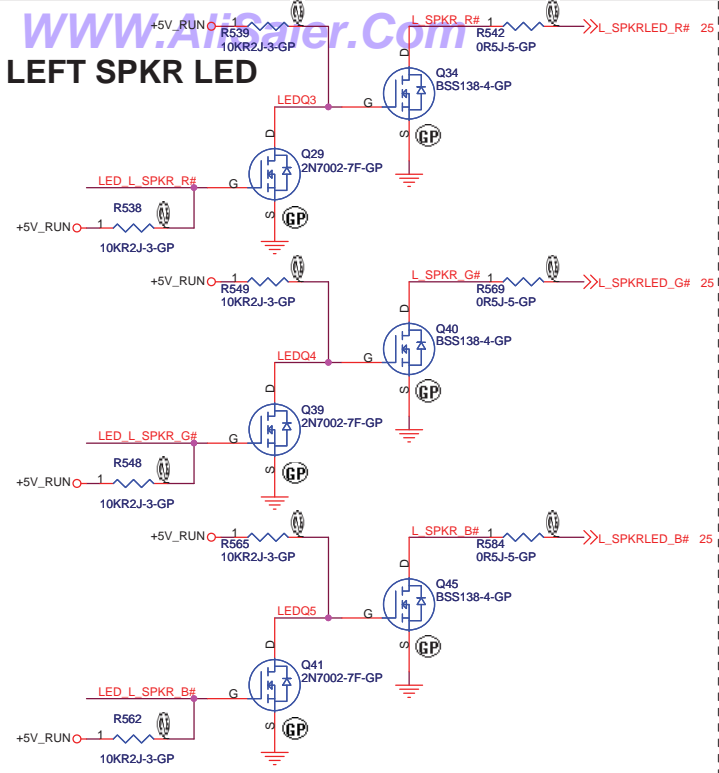
Bluetooth/ CIR/ Hall SW

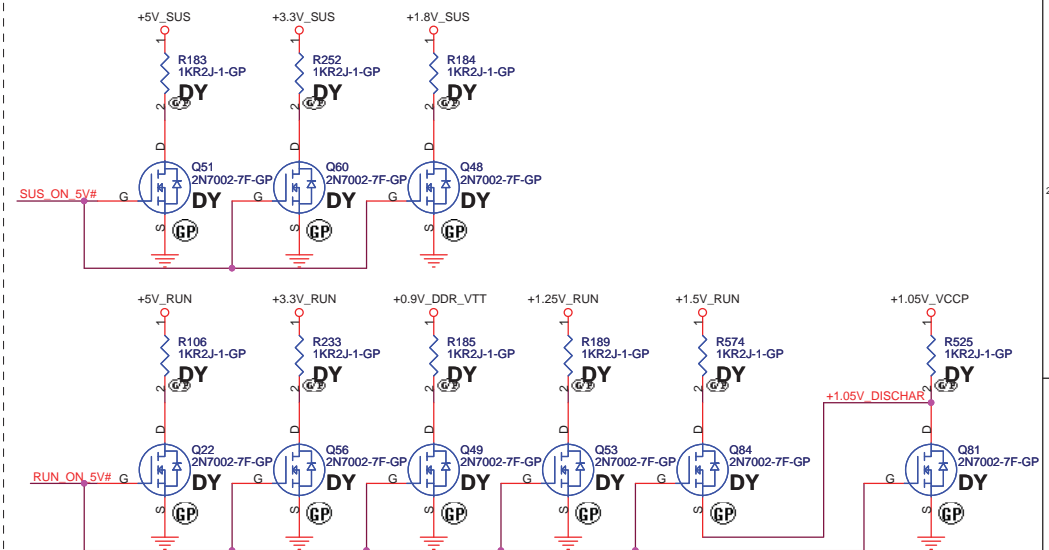
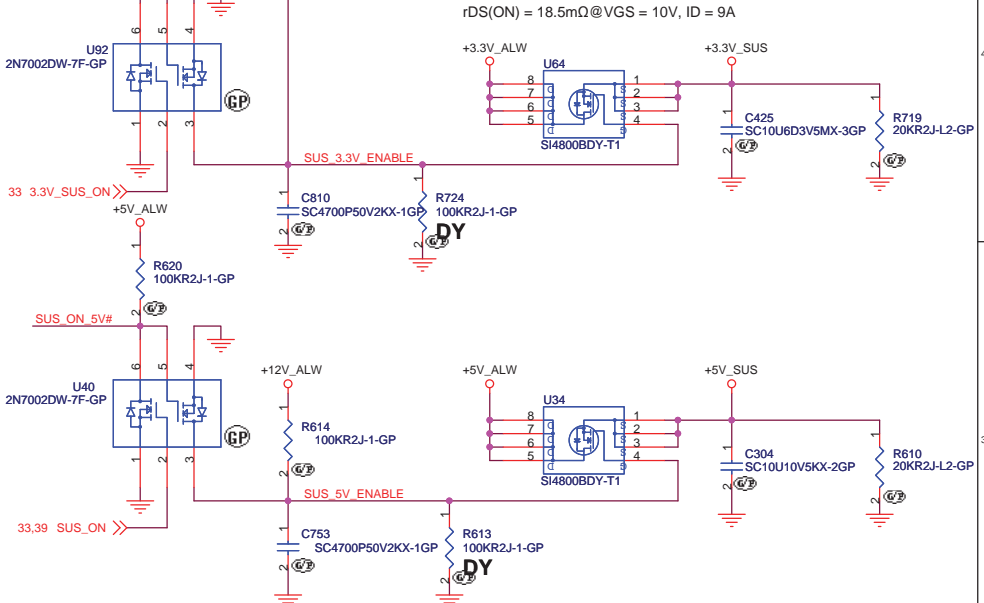
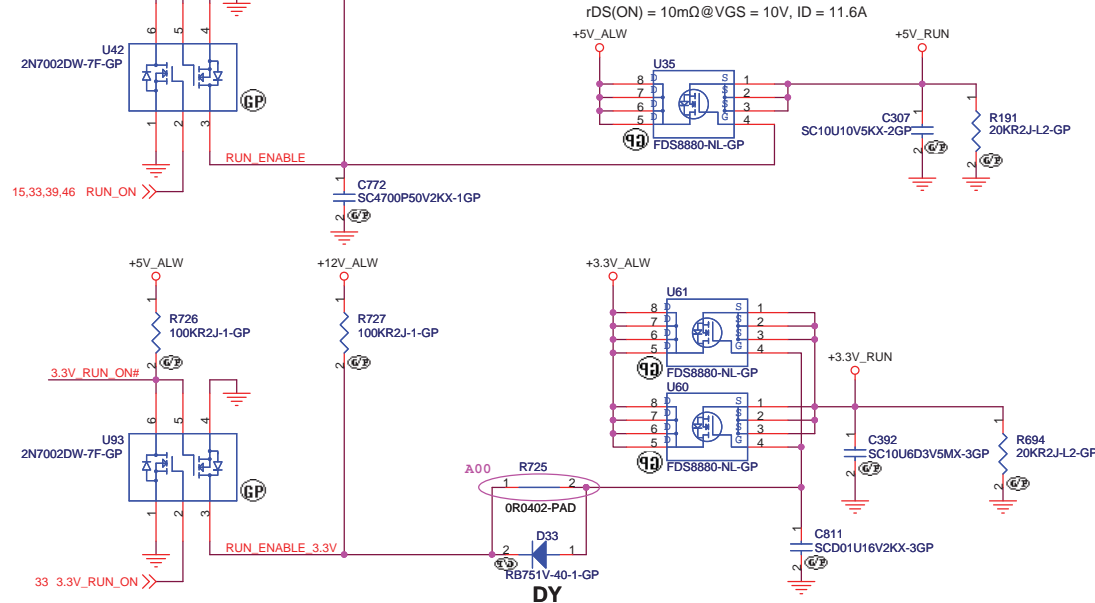


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Title				SPI FLASH / Bluetooth / CIR / LID			
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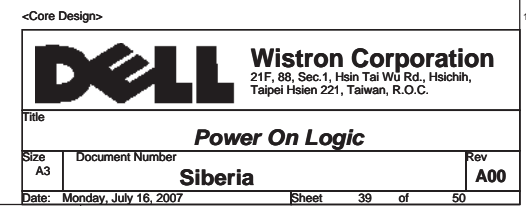


Reserve discharge path

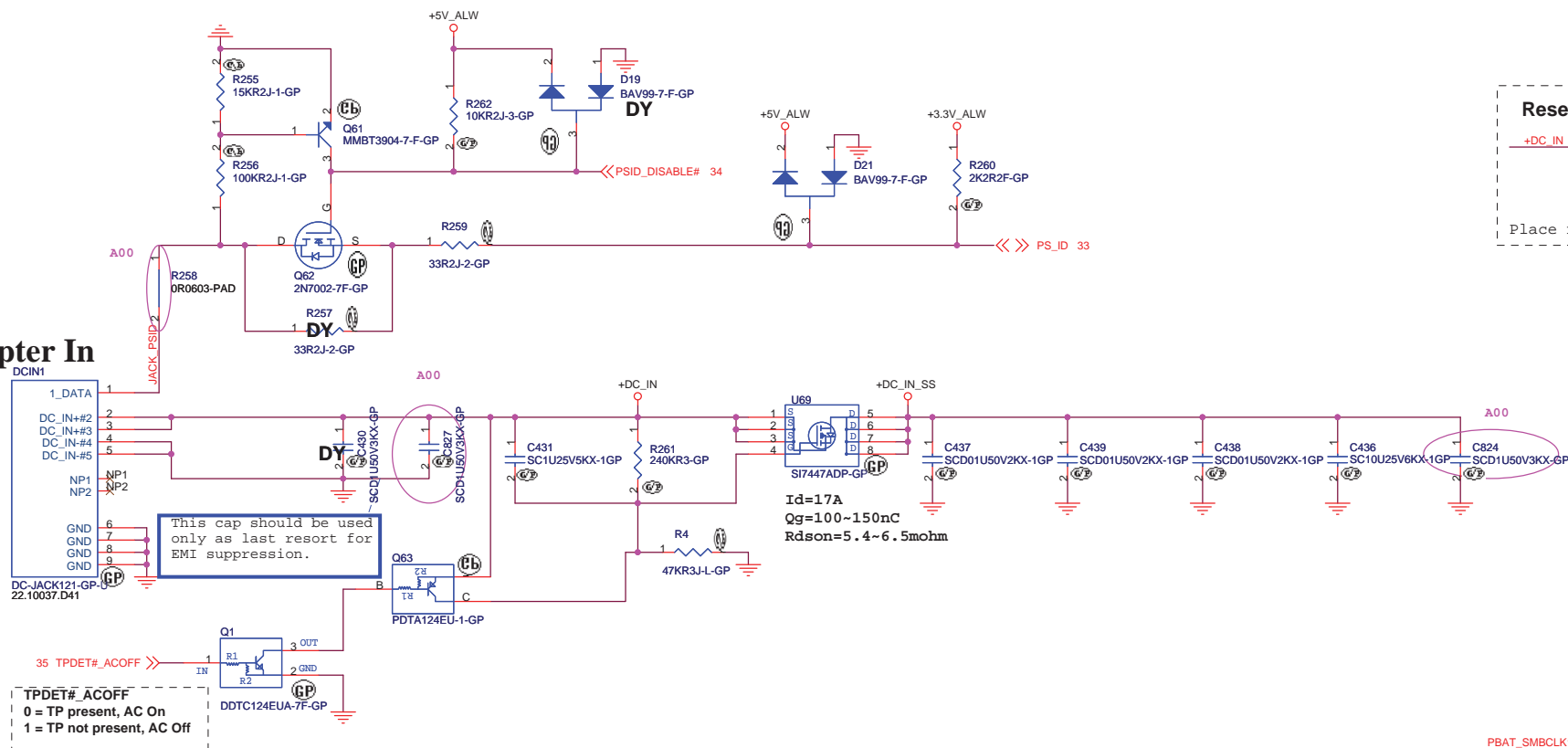
CRB 0.95:
Insures that +1.05_VCCP and +1.5_RUN ramp down together by discharging +1.5V_RUN into +1.05V_VCCP

<Core Design>

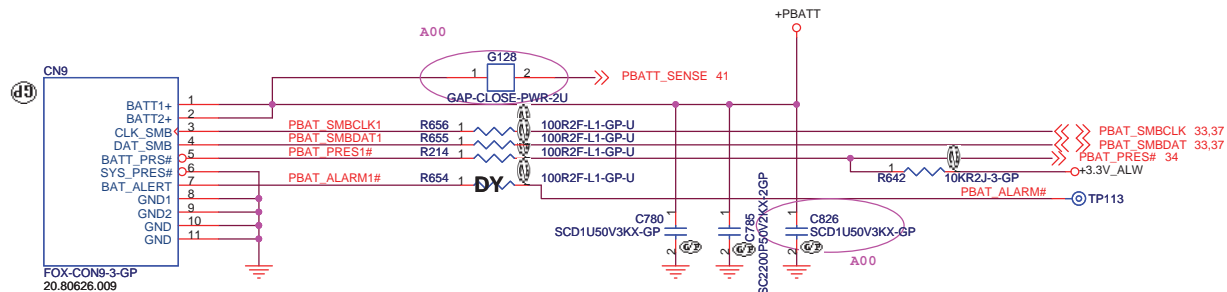
 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Power Plane Enable		
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Adapter In



Batt Connector



<Core Design>

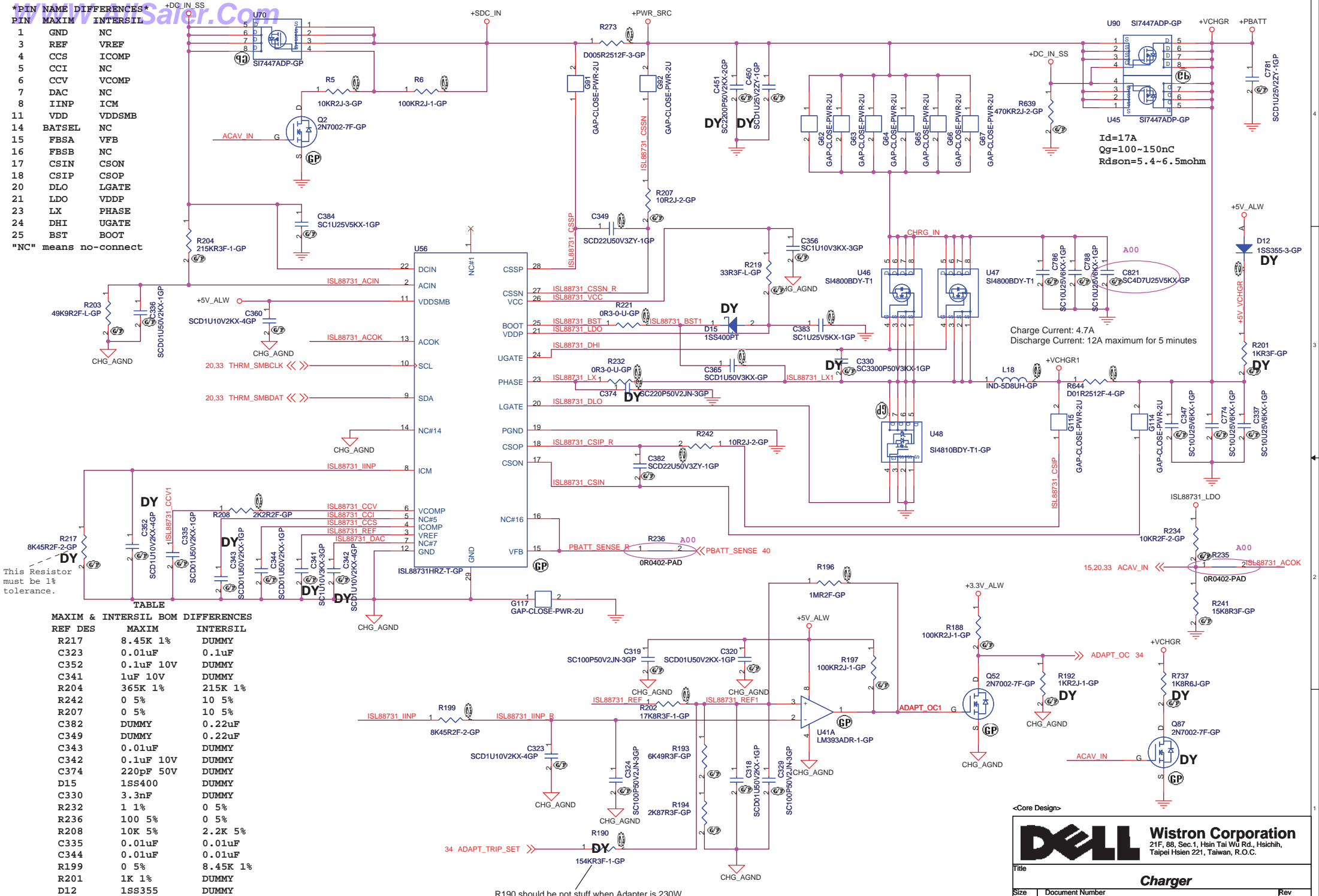


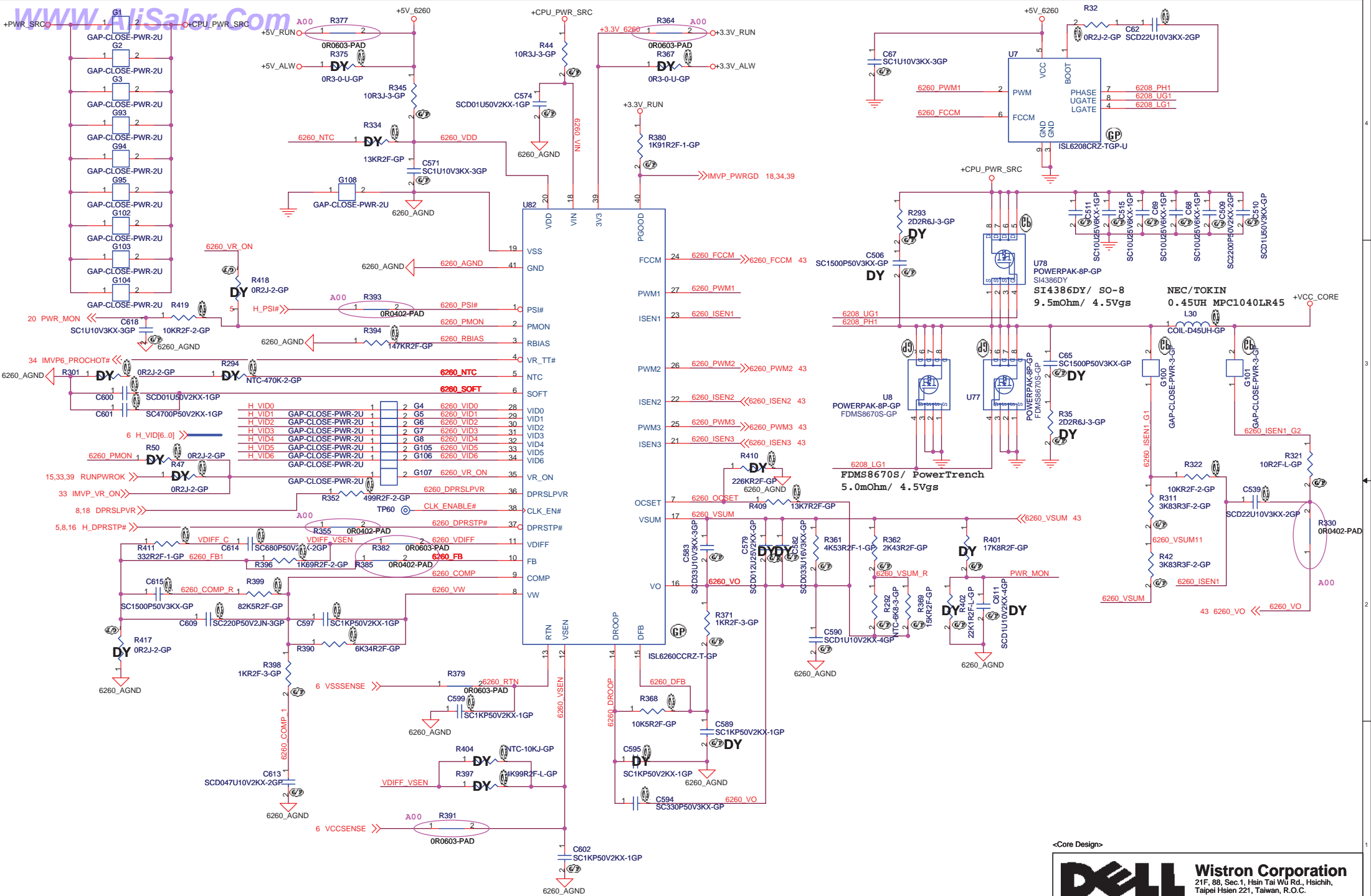
Title			DCIN / BATT CONN.		
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PIN NAME DIFFERENCES

PIN	MAXIM	INTERMIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSOP
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT

"NC" means no-connect



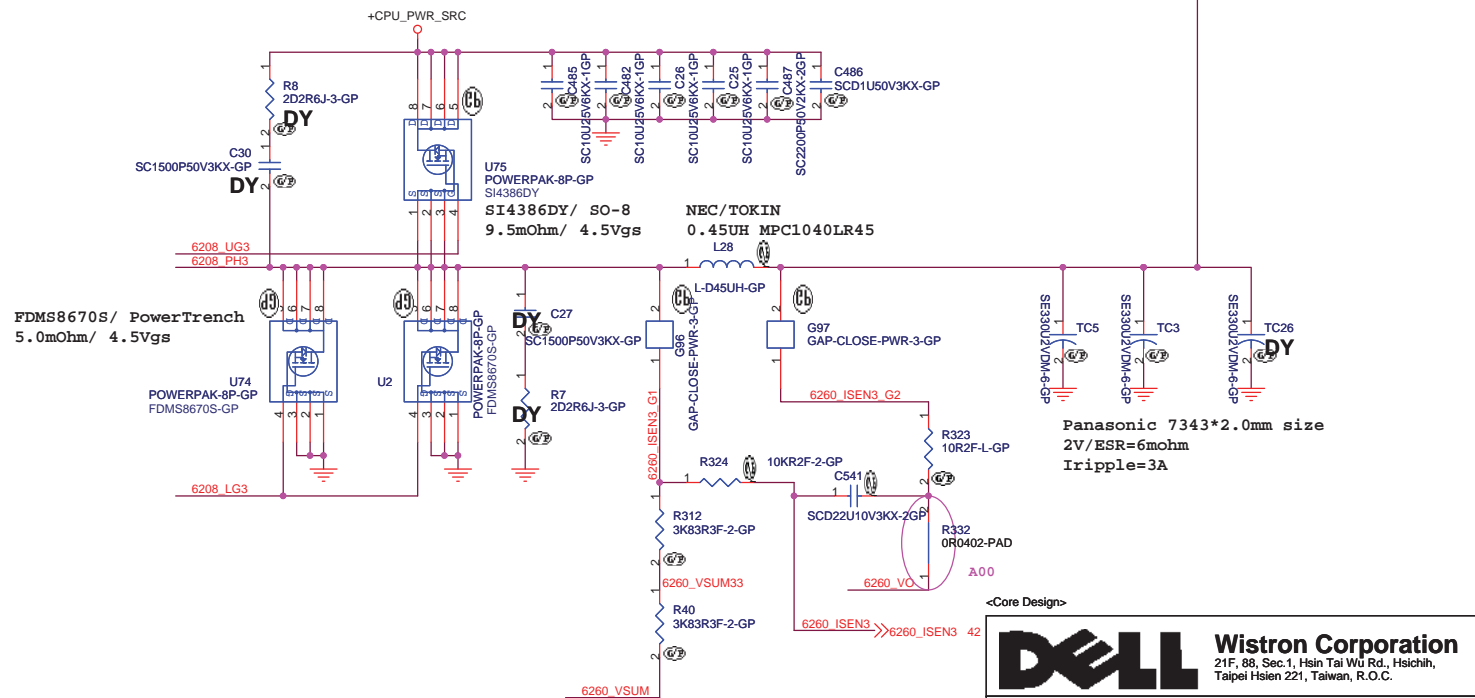
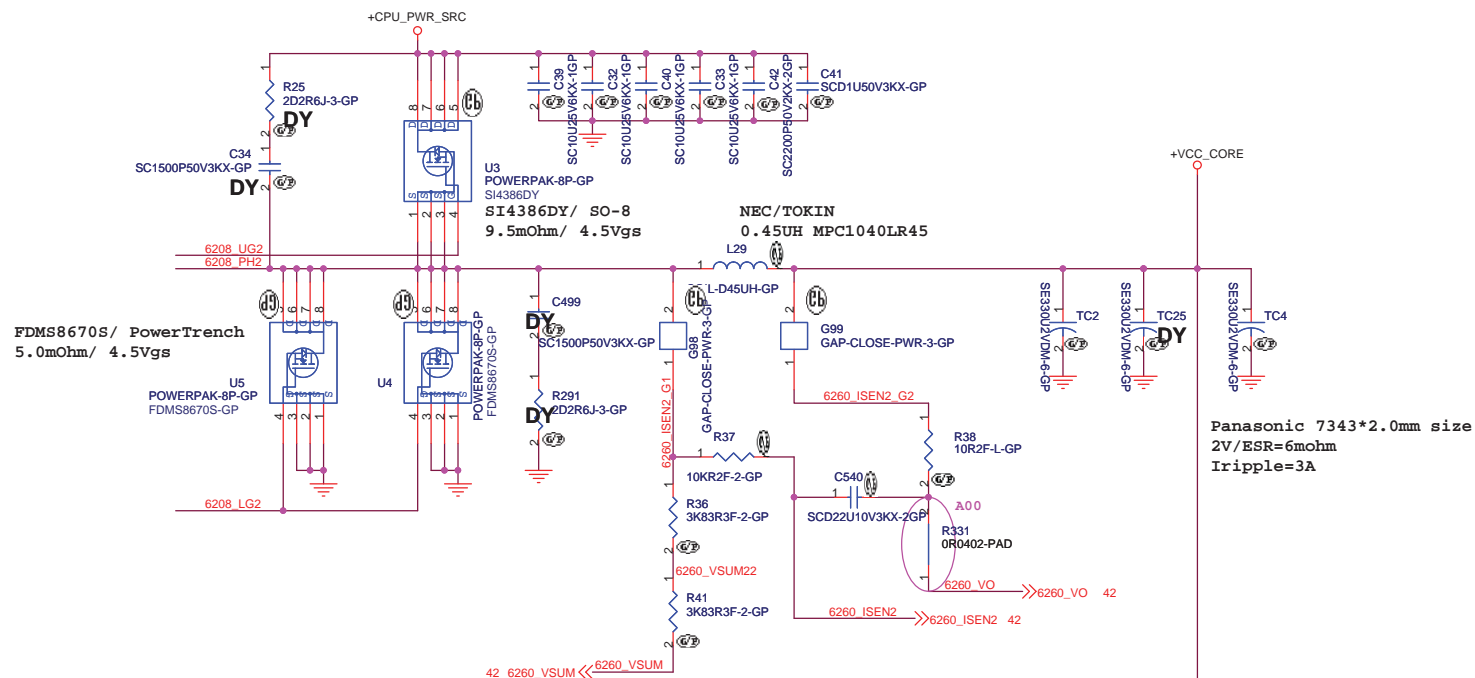
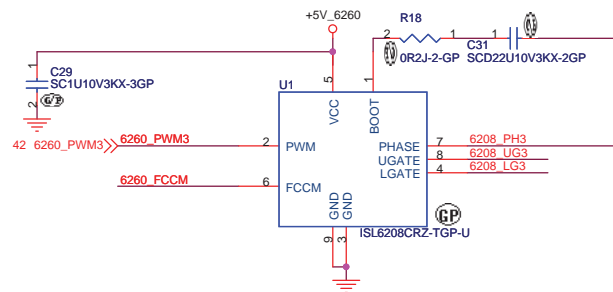
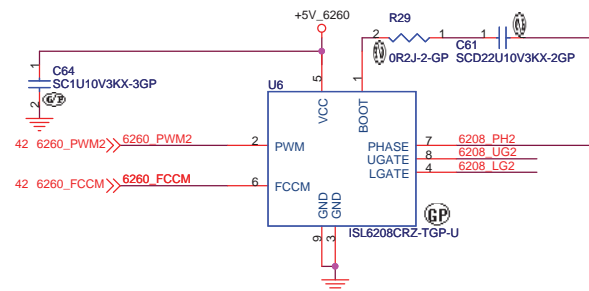


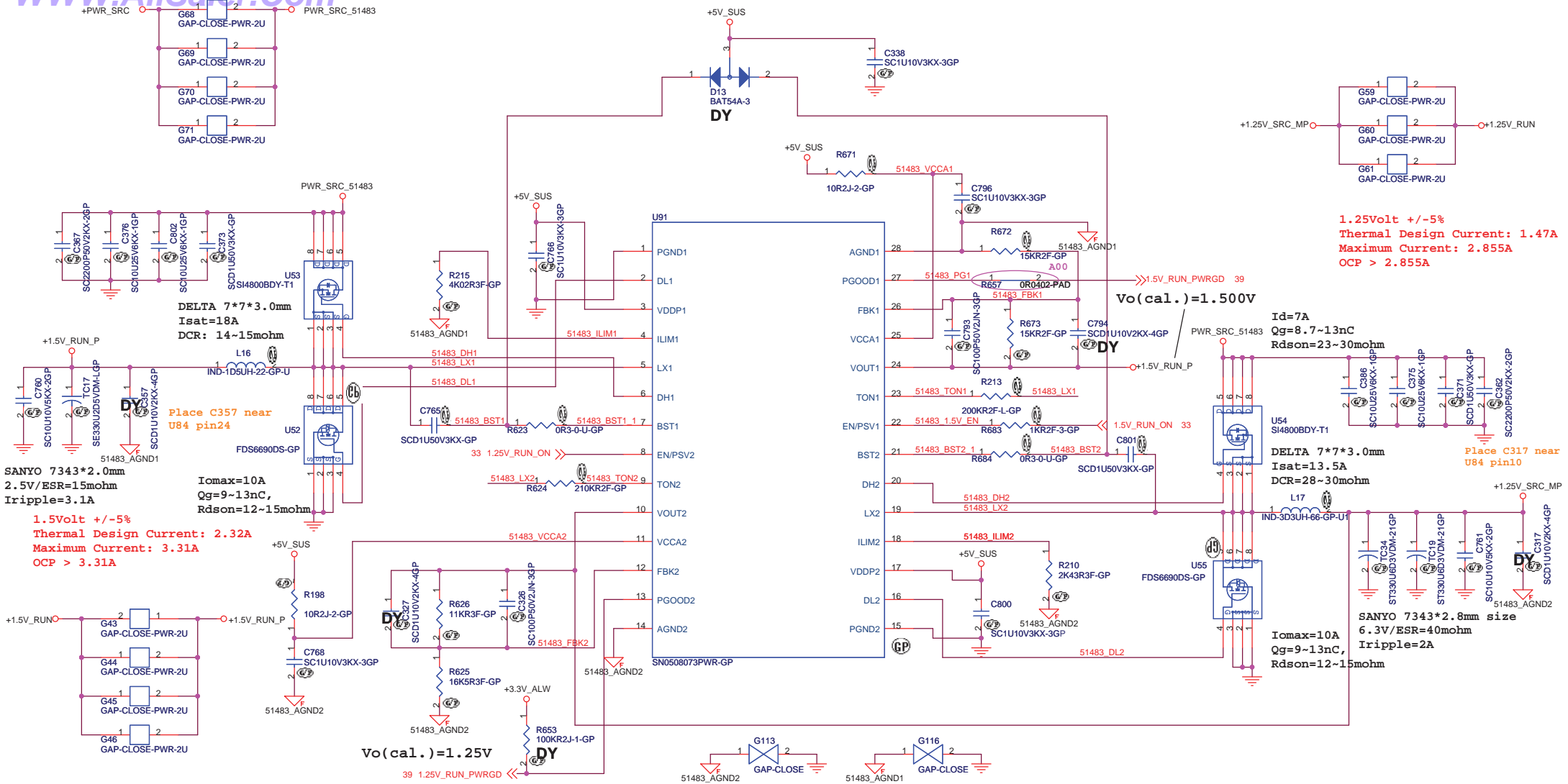
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU Vcore Power_1**

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$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{ds(on)}) + ((1/2 * L * f) * ((V_{in} - V_{out}) * V_{ou}) / V_{in})$$

$$V_{out} = (1 + (R_{top}/R_{bottom})) * 0.75$$

1.25Volt +/-5%
Thermal Design Current: 1.47A
Maximum Current: 2.855A
OCP > 2.855A

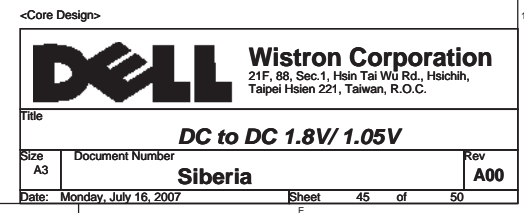
Place C317 near U84 pin10

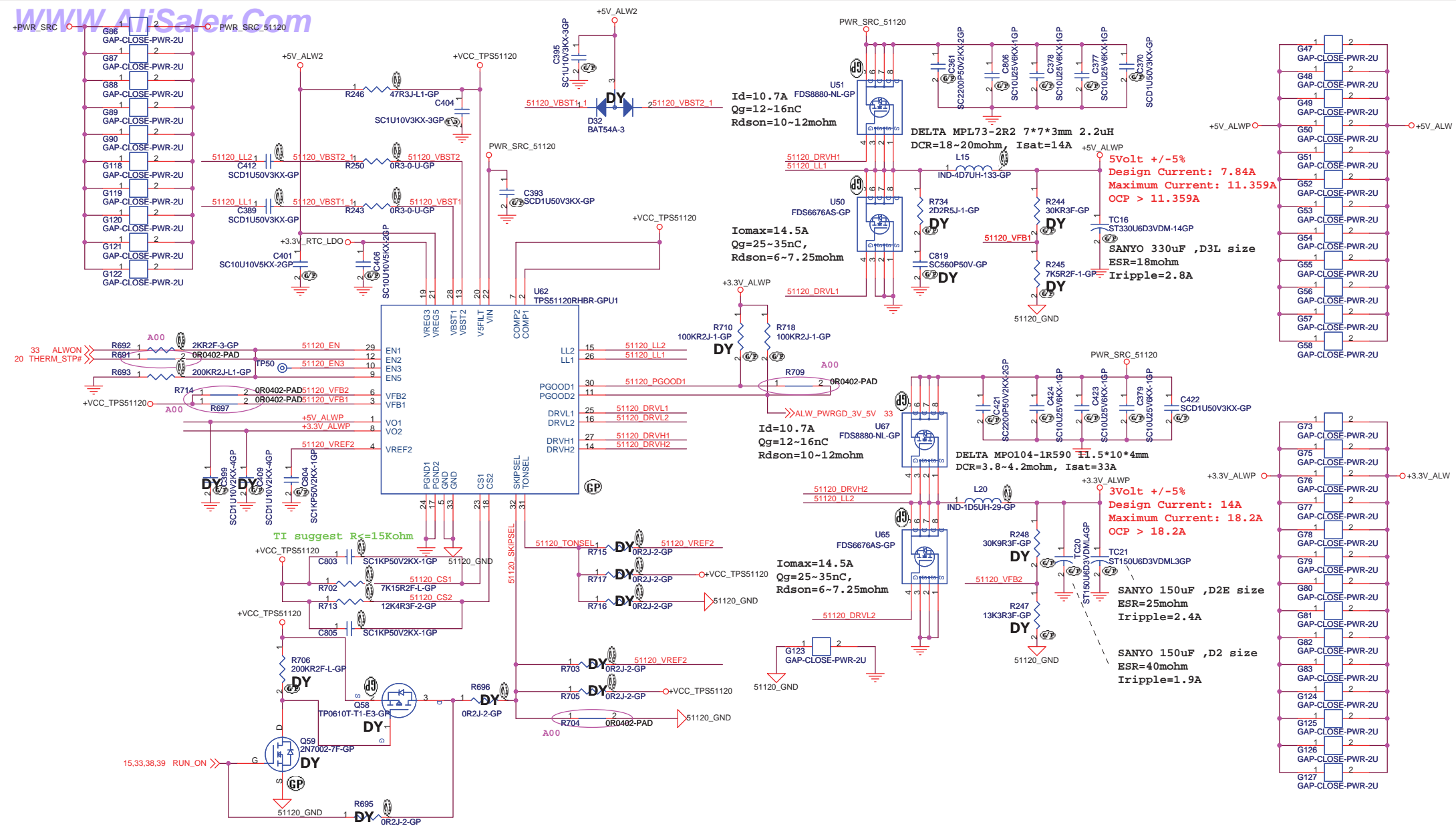
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Title: **DC to DC 1.5V/ 1.25V**

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	QNG	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Switchchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 ON

$$V_{out} = 1V * (R1 + R2) / R2$$

<Core Design>



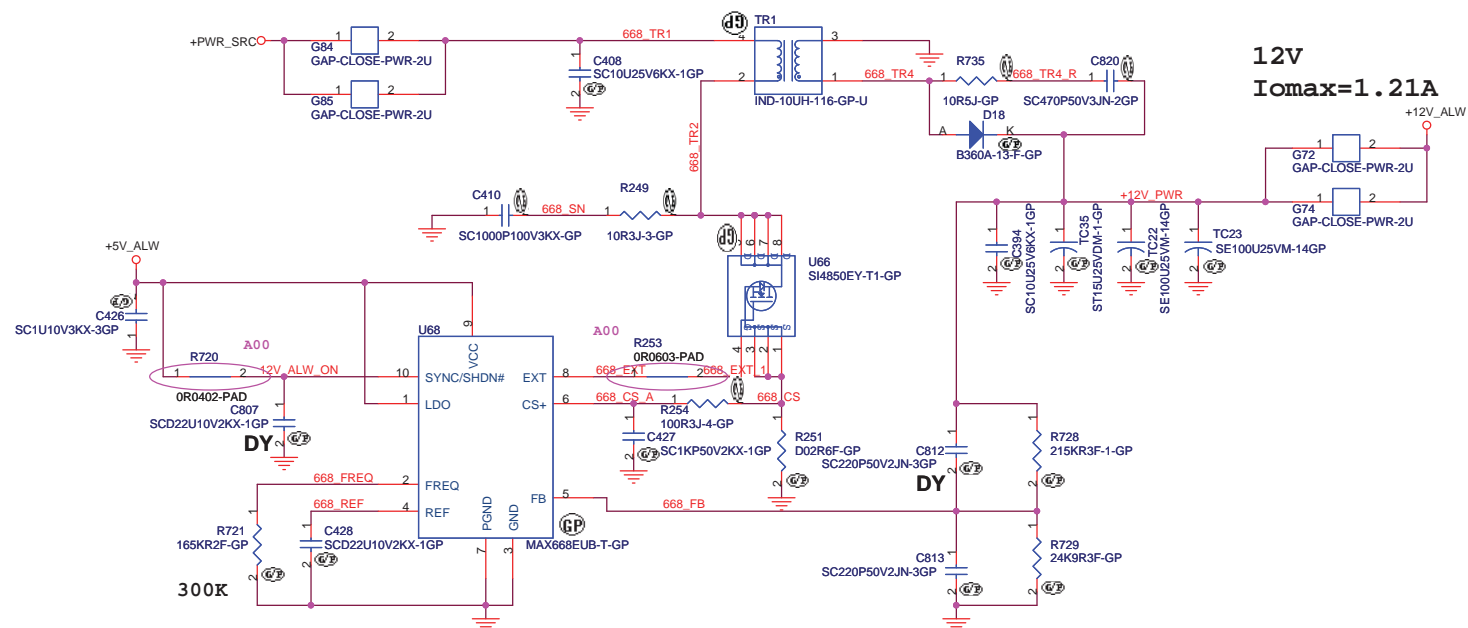
Title	
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DC to DC 3.3V / 5V

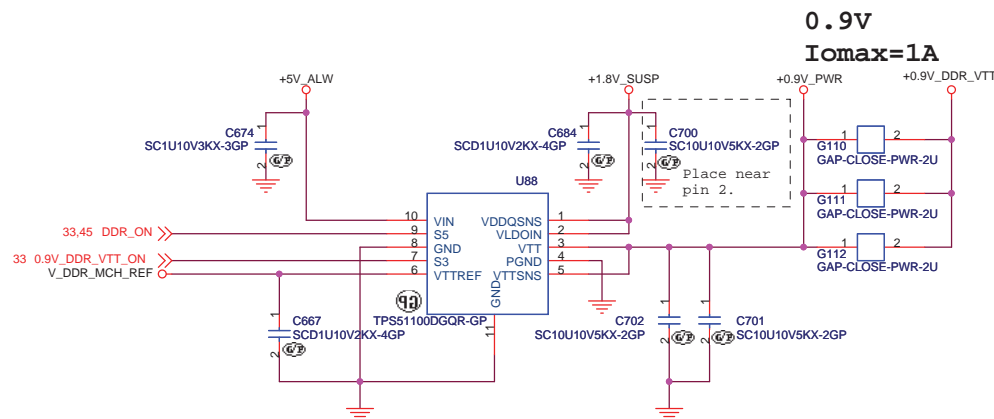
Size	Document Number	Rev
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12V
I_{omax}=1.21A

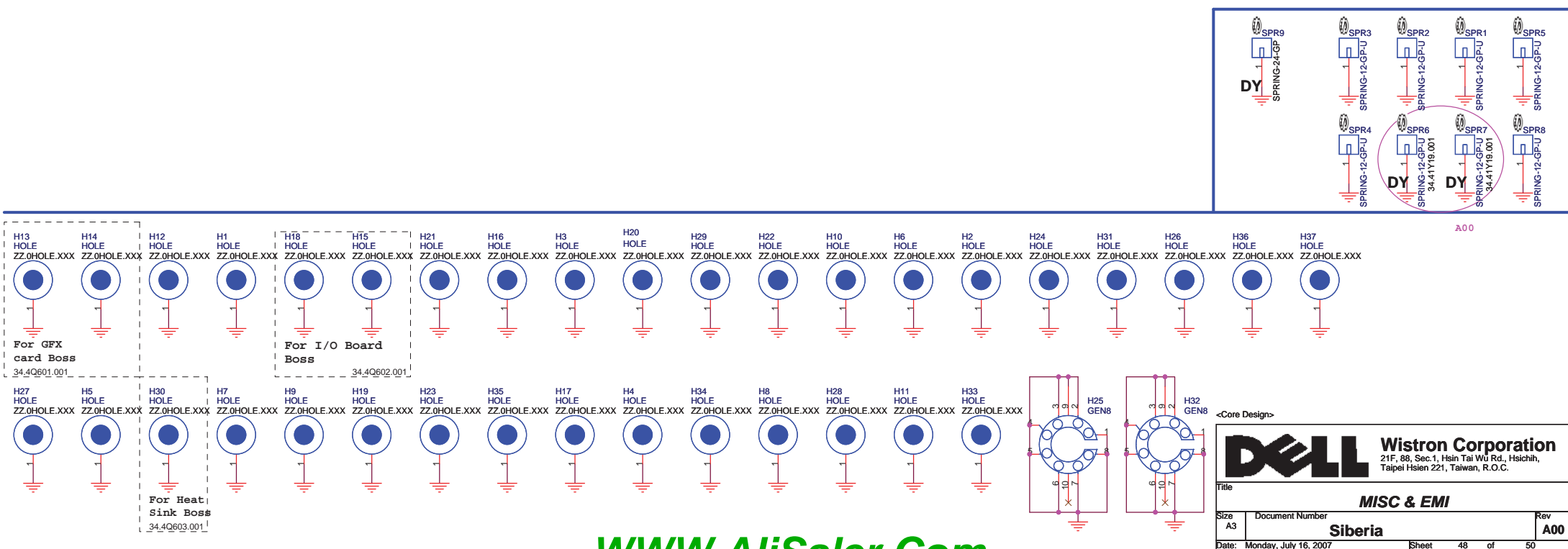
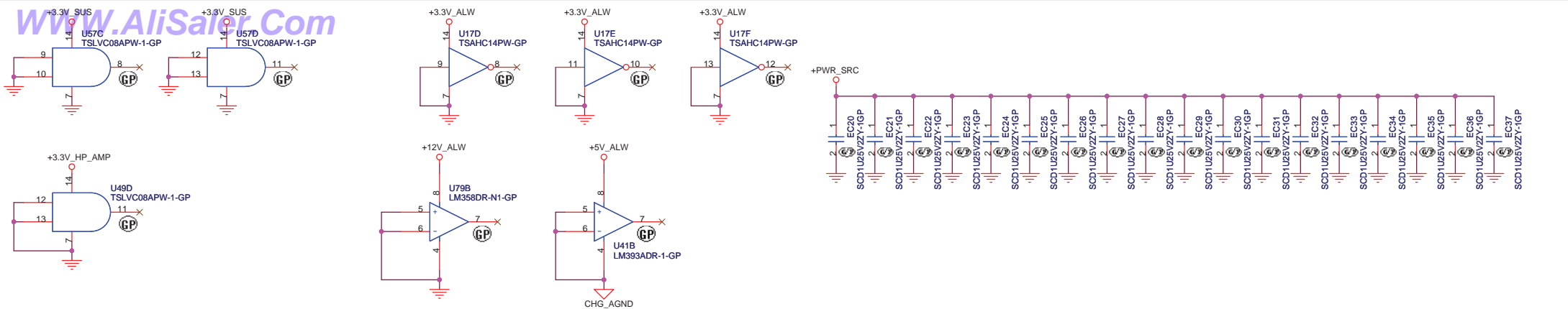


0.9V
I_{omax}=1A

<Core Design>



Title			DC to DC 12V / 0.9V		
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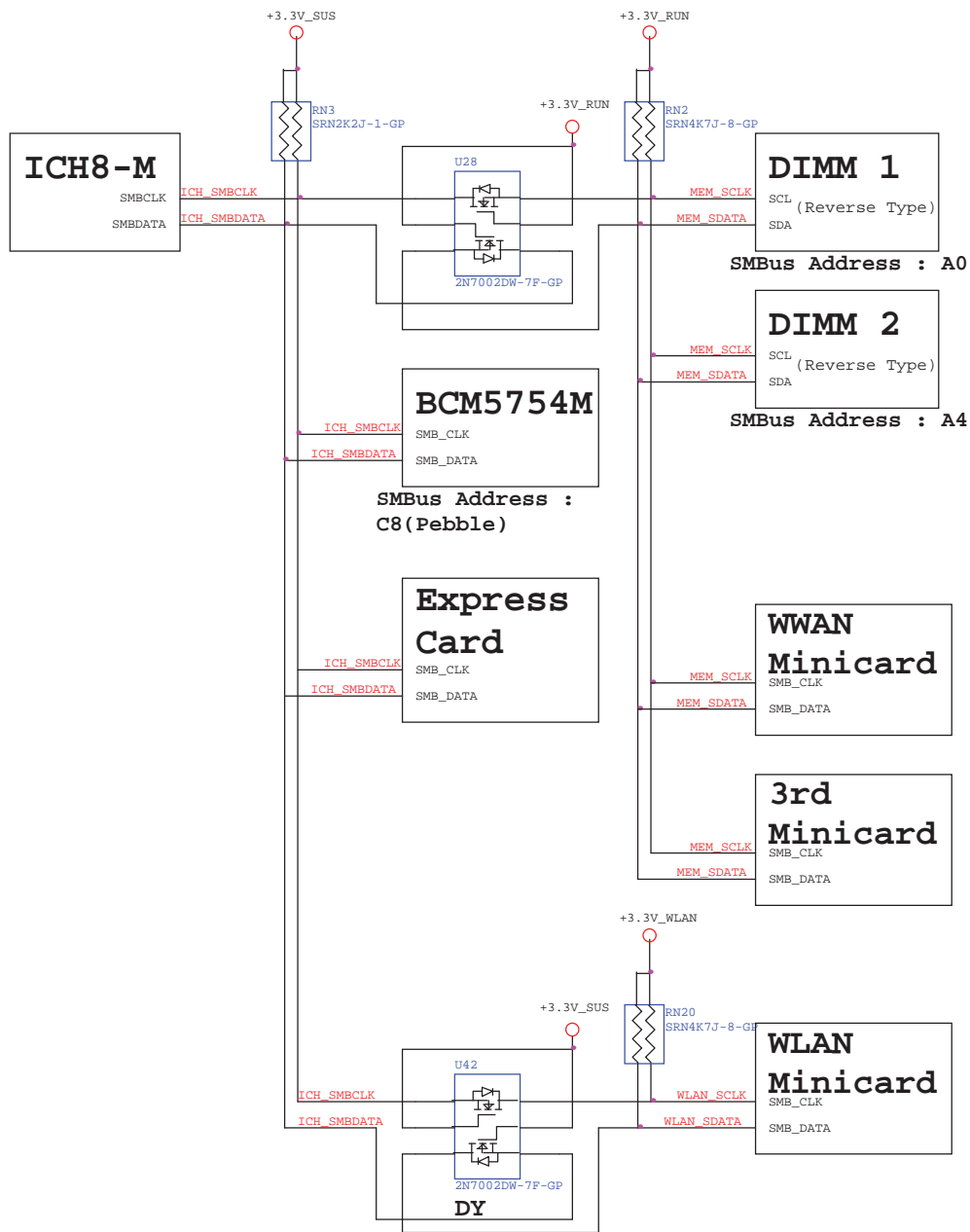
DELL

Title: **MISC & EMI**

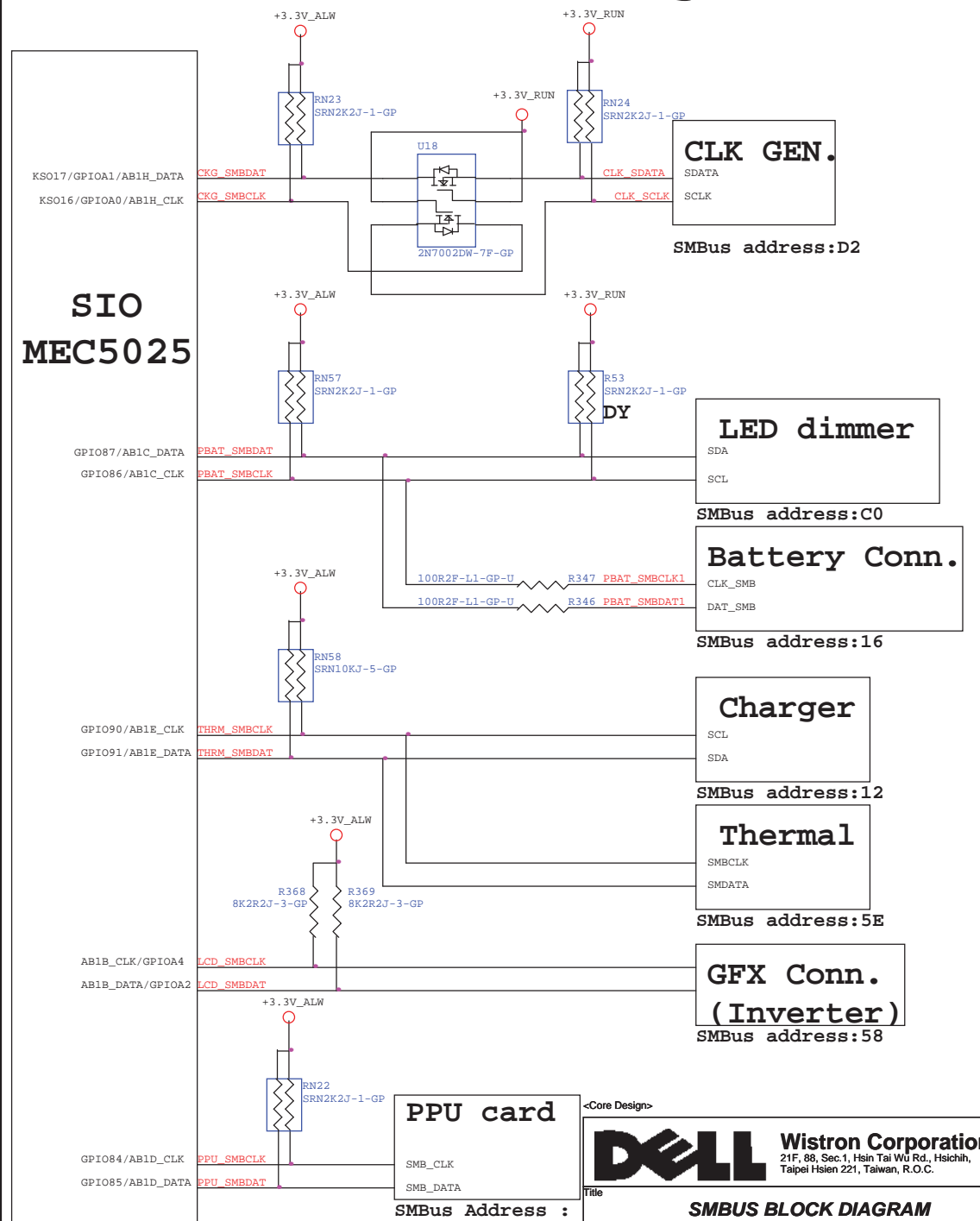
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ICH8 SMBus Block Diagram




KBC SMBus Block Diagram



DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/07/12	X02 to A00	1	19	Change C245 from 0.1U 0402 size to 1U 0603 size. (BITs ID: SCH159348)	Dell's command for ICH8 VREF power sequence glitch.	EE
		2	34	Populate R407 and non-populate R388.	Change board ID from X02 to A00.	EE
		3	36	Change U16 to vendor MXIC.	Because SST have shortage issue.	EE
		4	48	Non-populate SPR6, SPR7.(BITs ID: SCH159349)	Can't touch case.	EE
		5	4	Populate C661, C694 to 10p 50V 0402 size. Populate C693 to 8.2p 50V 0402 size.	Solution for 33MHz EMI issue.	EE
		6	4	Purge ICS CLK gen. and put Cypress at main source.	ICS CLK gen. has warn boot issue.	EE
		7	24	Add R739 10K ohm pull-high to +3.3V_RUN.(SCH159171)	For audio AUD_EAPD#.	EE
		8	41	Remove C354 and C358, add C821 as 4.7U 25V 0805.		EMI
		9	15	Add C823 as 0.1U 50V 0603 for +GFX_PWR_SRC.		EMI
		10	40	Add C827 as 0.1U 50V 0603 for +DC_IN.		EMI
		11	40	Add C824 as 0.1U 50V 0603 for +DC_IN_SS.		EMI
		12	40	Add C826 as 0.1uF for +PBATT. Change R218 to close gap.		EMI
		13	28	Populate C434 and C435 as 47pF, non-populate R265. Change L21 to 2500ohm bead.		EMI
		14	27	Change R285 from 1.24K ohm 5% to 1.27K ohm 1%. Change C449 and C461 to 47pF, C447 to 4.7uF.		EMI
		15	31	Non-pop R588, R590.	Command from DELL wireless team.	EE
		16		Change many 0ohm resistors to wire pad.		EE

-Core Design-



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HISTORY from X00 to X01

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